

GRAPHENE NANORIBBON FIELD EFFECT TRANSISTOR FOR DIGITAL IC APPLICATIONS

Dinh Sy Hien¹, Le Hoang Minh², Nguyen Thi Luong²

¹Ho Chi Minh City University of Science, Vietnam

²Ho Chi Minh City University of Technology and Education, Vietnam

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ABSTRACT

Graphene has been one of the most vigorously studied materials. Graphene has attracted considerable attention from the scientific community due to its excellent electronic properties. The impressive properties of graphene make it an attractive candidate for electronic devices of the future. This work explores whether graphene fulfills the promises raised by the extraordinary material properties. The opening of bandgap in grapheme) nanoribbons by quantum confinement holds promise for digital electronic device applications. We report model and device performance of low band gap grapheme nanoribbon field effect transistors (GNRFET). For the substantial current modulation at room-temperature, sub-10 nm grapheme nanoribbon widths are required. This paper also presents typical current-voltage characteristics of the GNRFET for demonstration. We have proposed a way to calculate the on-off current ratio for GNRFET having channel length of 10 nm and width of 1 nm. Scaling of channel length of GNRFET below 10 nm is observed.

Key words: Graphene nanoribbon FET; narrow band gap; on-off current ratio; Nano electronics; non-equilibrium Green's function.

1. INTRODUCTION

Graphene has been one of the most vigorously studied materials since its inception in 2004. Graphene has attracted considerable attention from the scientific community due to its excellent electronic properties, as high mobility even at room temperature and at high doping concentration, high thermal conductivity, and its interesting optical properties.

High intrinsic carrier mobility [1], high thermal conductivity [2], and the one atomic thick structure are one of some properties that make grapheme an appealing material for high speed electronics [3]. However, the absence of a band gap in 2D graphene limits

the on-off current ratio of grapheme field effect transistors (GFET) to 10 at room temperature, which is lower than the requirement for digital electronics applications. Confining the carriers in graphene in lateral dimension by fabricating graphene nanoribbons (GNR) can induce a band gap whose magnitude depends on the width of the GNR, thus enabling higher on-of current ratio. The confinement induced band gap can be approximated by the formula [4]:

$$\Delta E(W) = \frac{h v_0}{2W} = \frac{2.07 \text{ (eV} \cdot \text{nm)}}{W \text{ (nm)}} \quad (1)$$

Where $v_0 = 10^6 \text{ m/s}$, h is Plank constant, $4.14 \times 10^{-15} \text{ eVs}$ and W is expressed in nanometres.

Top-down approaches for fabricating GNR using graphene flakes and e-beam lithography lead to GNRs as narrow as 14 nm [5]. The lowest GNR width attainable with this approach is limited by the resolution of e beam lithography and increased line edge roughness (LER) at the resolution limit.

Randomly dispersed GNR narrower than 10 nm with atomically smooth edges have been formed by unzipping carbon nanotube (CNT) [6] or by ultrasonication of exfoliated graphite in an appropriate solution [7]. However, this method suffers the same fundamental problems that have limited up to now – the technological applicability of randomly deposited CNTs in the fabrication of large-scale electronic devices, that is, the lack of accurate and deterministic placement of CNTs with controlled diameter and chirality, as well as with high CNT area density.

Recently, G. Liu et al. [8] have developed a process enabling to fabricate arrays of epitaxial graphene nanoribbons with the smooth edge GNR width as low as 10 nm by e-beam lithography on graphene epitaxial grown on SiC wafers. These are the narrowest epitaxial graphene nanoribbons on SiC fabricated to date.

With promising progresses on fabricating a narrow graphene layer, graphene electronics has been a topic of strong research interests. A narrow strip of graphene, graphene nanoribbon can be metallic or semiconductor, depending on its structure [9]. An exceptionally high mobility (10000 cm²/Vs) of graphene and GNRs have been demonstrated experimentally [10] and theoretically [11], which leads to the promise of near ballistic transport in a nanoscale graphene nanoribbon field effect transistor (GNRFET). The channel geometry can be defined by lithography. The concept of all graphene circuits, in which GNRFETs are connected by metallic GNR interconnects has been proposed [4]. A Quite recently great progress has been achieved in fabricating graphene field effect devices [12, 13]. There

has been an excellent review published recently with emphasis on basic science of graphene FET [14].

In this work, a comprehensive study on the scaling behaviours of GNRFETs is performed by solving an atomic quantum transport equation based on the non-equilibrium Green's function (NEGF) formalism. The dependence of the current-voltage characteristics on the channel length are studied for top-gate GNRFET geometry.

2. TOP-GATE DEVICE, SIMULATION METHOD AND RESULTS

2.1 Simulated Device Structure with Top-Gate Geometry

We simulated GNRFETs with top-gate geometry at room temperature ($T = 300$ K) to explore the effect of channel geometry on the performance of GNRFETs. Fig. 1 shows top-gate GNRFET which has the advantage of easy fabrication using present IC fabricated technology (planar technology). The top-gate GNRFET having a channel of a highly-doped, n-type with NH₃ doping concentration is also assumed for suppressing Schottky effect in the source-semiconducting-drain contacts of the device.

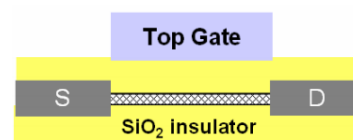


Figure 1. Simulated device structure with top-gate geometry: the channel materials are semiconducting GNR. The source and drain contacts are GNR metals, and two ends of the GNR channel have been heavily doped.

The nominal device parameters are as follows. The SiO₂ gate oxide thickness $t_{ox} = 2$ nm and the relative dielectric constant $\epsilon_r = 3.9$. The GNR channel has armchair edges as shown in Fig. 2. The armchair edge GNR channel has a width of 1 nm, which results in a band gap $E_g = 0.8$ eV while using empirical formula of $E_g = 0.8/W$. The

channel length is 10 nm. A power supply voltage of $VDD = 0.8$ V. The nominal parameters are varied to explore different scaling issues.

2.2 Quantum transport

The DC characteristics of GNR-FET are simulated by solving Schrodinger equation using the non-equilibrium Green's function formalism self-consistently with a Poisson equation. Ballistic transport is assumed. A tight binding Hamiltonian is used to describe an atomistic physical observation of the GNR channel. The size of the Hamiltonian is $N \times N$, where N is the number of carbon atoms in the channel.

The flow of current is due to the difference in potentials between the source and the drain, each of which is in a state of local equilibrium, but maintained at different

electro-chemical potentials $\mu_{1,2}$ and hence with two distinct Fermi functions:

$$f_1(E) \equiv f_0(E - \mu_1) = \frac{1}{\exp[(E - \mu_1)/k_B T] + 1} \quad (2)$$

$$f_2(E) \equiv f_0(E - \mu_2) = \frac{1}{\exp[(E - \mu_2)/k_B T] + 1} \quad (3)$$

By the applied bias V : $\mu_2 - \mu_1 = -qV$. Here, E- energy, k_B - Boltzmann constant, T- temperature.

The density matrix is given by

$$\rho = \int_{-\infty}^{+\infty} \frac{dE}{2\pi} G^n(E) = \int_{-\infty}^{+\infty} \frac{dE}{2\pi} [A_1(E)f_1(E) + A_2(E)f_2(E)] \quad (4)$$

The current ID flows in the external circuit is given by Landauer formula:

$$I_D = (q/h) \int_{-\infty}^{+\infty} dE T(E) (f_1(E) - f_2(E)) \quad (5)$$

The quantity $T(E)$ appearing in the current equation (5) is called the transmission function, which tells us the rate at which electrons transmit from the source to the drain contacts by propagating through the device. Knowing the device Hamiltonian [H] and its

coupling to the contacts described by the self-energy matrices $\Sigma_{1,2}$, we can calculate the current from (5). For coherent transport, one can calculate the transmission from the Green's function method, using the relation

$$T(E) = \text{Trace}[\Gamma_1 G \Gamma_2 G^+] = \text{Trace}[\Gamma_2 G \Gamma_1 G^+] \quad (6)$$

The appropriate NEGF equations are obtained:

$$G = [EI - H - \Sigma_1 - \Sigma_2]^{-1}, \Gamma_{1,2} = i[\Sigma_{1,2} - \Sigma_{1,2}^*]$$

$$A_1(E) = G \Gamma_1 G^*, A_2(E) = G \Gamma_2 G^*$$

$$G^n(E) = [A_1]f(E) + [A_2]f(E) \equiv i[G - G^+] = [A_1] + [A_2] \quad (7)$$

Where H is an effective mass Hamiltonian, I is an identity matrix of the same size, $\Gamma_{1,2}$ are the broadening functions, $A_{1,2}$ are partial spectral functions, $A(E)$ are spectral functions, G^n is a correlation function.

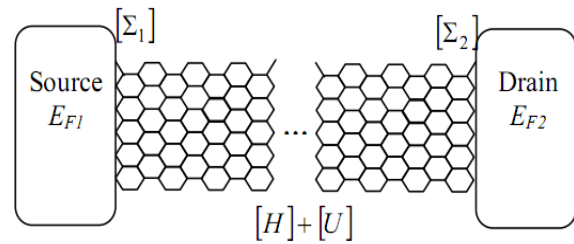


Figure 2. The schematic sketch of an armchair edge GNR channel with the source and drain contacts. The quantities used in the NEGF formalism are also shown.

2.3 Simulation Results and Discussion

We next study on the effect of power supply voltages. The output characteristics in Fig. 3 show typical linear and saturation regimes. When VG is increased saturation current is increased due to a larger voltage drop between the gate and the source contacts and a larger energy range for carrier injection from the source contact into the channel.

The switching on characteristics is described by simulating the GNR-FET transconductance. The transconductance,

$$g_m = \frac{\partial I_D}{\partial V_G}$$

is the ratio of current variation to the gate voltage at on state. Considering the ID-VD characteristics of the GNR-FET, the

following observations were made. First, the transconductance depends on the gate voltage. Second, as the gate voltage decreases and approaches to 0.1 V, the transconductance decreases. The maximum transconductance of the GNFET can be computed as

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{1 \times 10^{-6} \text{ A}}{0.7 \text{ V}} = 1.4 \mu\text{S}$$

The GNFET transconductance is existing, but too small.

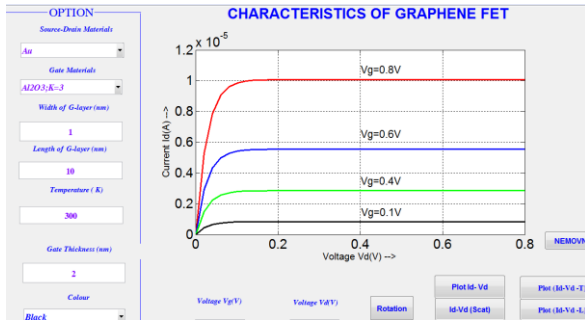


Figure 3. The ID-VD characteristics of the top-gate GNFET at different gate voltage, $V_G = 0.1 \text{ V}, 0.4 \text{ V}, 0.6 \text{ V}, 0.8 \text{ V}$ (bottom to up).

The ID versus VG characteristics for the top-gate GNFET is plotted in Fig. 4. Increasing gate voltage leads to an exponential increase of the drain current.

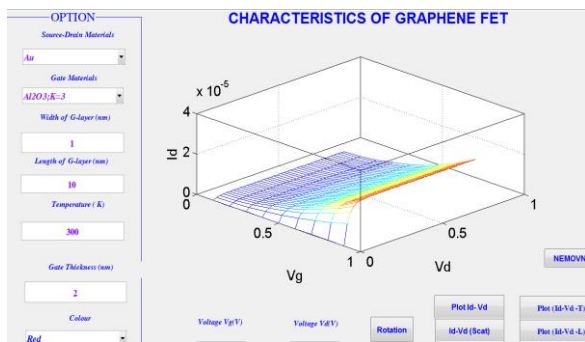


Figure 4. The 3D plot of ID-VD characteristics of the top-gate GNFET versus VG, where the length of the gate is $LG = 10 \text{ nm}$.

Fig. 5 shows the 3D plot of ID-VD characteristics of the GNFET versus the temperature, T. It can be noted that as the temperature increases the saturated drain current gradually increases. We also observe that the off current is about $1 \times 10^{-9} \text{ nA}$ at very low temperature and the low gate voltage, $V_G = 0.1 \text{ V}$. From Fig. 3 and Fig. 5 we can calculate on-off current ratio, $I_{on}/I_{off} = 1 \times 10^{-5} \text{ nA} / 1 \times 10^{-9} \text{ nA} = 104$. The reason is

that the band gap of the GNR channel strongly depends on its width, which significantly affects to the on-off current ratio.

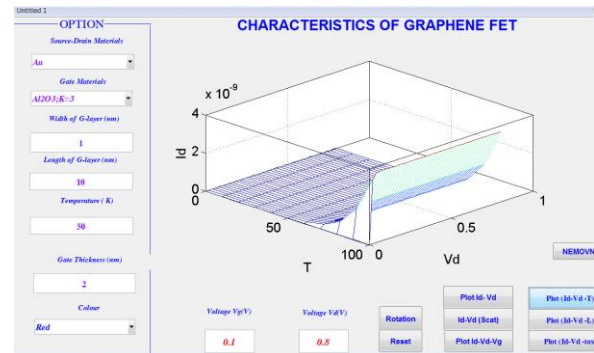


Figure 5. The 3D plot of the ID-VD characteristics of the top-gate GNFET versus temperature. The GNFET parameters are: the gate length is $LG = 10 \text{ nm}$, the gate thickness is $t_{ox} = 2 \text{ nm}$, at the gate voltage, $V_G = 0.1 \text{ V}$.

The effect of the channel length scaling on the device characteristics is observed. ID-VD characteristics of GNFET versus the length of the gate layer at room temperature are shown in Fig. 6. Apparently, as the length of the GNFET decreases, the saturated drain current gradually increases. A Significant increase of the drain current is observed when the channel length is scaled below 10 nm. For channel length of 15 to 20 nm, ID-VD curves can be obtained and the difference in length results in only a little change in ID-VD curves. The reason is that because the GNR channel operates as metallic material.

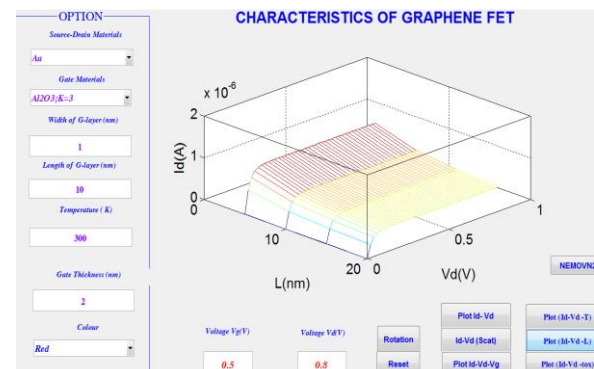


Figure 6. The 3D plot of the ID-VD characteristics versus the gate length of the top-gate GNFET at room temperature, $T = 300 \text{ K}$. The parameters of GNFET: material, the gate thickness, $t_{ox} = 2 \text{ nm}$.

The effect of the gate thickness scaling on the device characteristics is observed. ID-VD characteristics of GNRFET versus the gate thickness at room temperature are shown in Fig. 7. Apparently, as the gate thickness of the GNRFET decreases, the saturated drain current gradually increases.

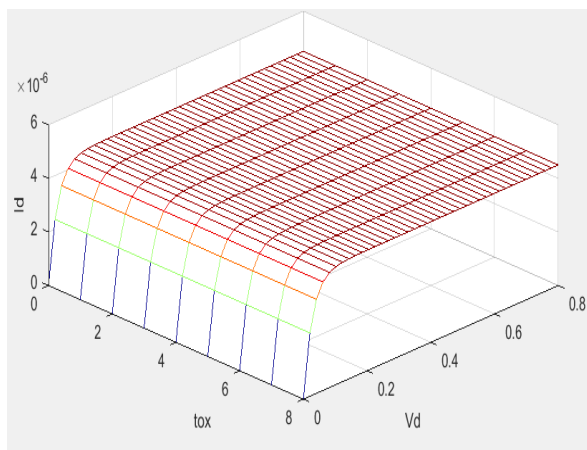


Figure 7. The 3D plot of the ID-VD characteristics versus the gate thickness of the top-gate GNRFET at room temperature, $T = 300$ K.

3. CONCLUSIONS

A model for the top-gate GNRFET using NEGF written in GUI of Matlab has been reported. The current-voltage characteristics of the top-gate GNRFET have been simulated. Typical simulations which are then successfully performed for parameters of the GNRFET or the electronic transport of GNRFET has been investigated. The model is able to accurately describe not only ID-VG, and ID-VD characteristics of the GNRFET, but also the effects of channel materials, gate materials, size of the GNRFET, and temperature on the characteristics. The obtained results indicate that the performance of GNRFET in terms of on-off current ratio is apparent in narrow ribbons. We have proposed a way to calculate the on-off current ratio for GNRFET having a channel length of 10 nm and width of 1 nm. A Significant increase of the drain current of GNRFET is also observed when the channel length is scaled below 10 nm. The simulation program has been integrated in a quantum simulator NEMO-VN2 [15].

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Corresponding author:

Le Hoang Minh

Ho Chi Minh City University of Technology and Education

Email: minhhlh@hcmute.edu.vn