

NEMO-VN2-2019 AN USEFUL SIMULATION TOOL FOR EMERGING NANO ELECTRONIC DEVICES

Dinh Sy Hien¹, Le Hoang Minh², Nguyen Thi Luong²

¹Ho Chi Minh City University of Science, Vietnam

²Ho Chi Minh City University of Technology and Education, Vietnam

Received 23/12/2019, Peer reviewed 19/1/2020, Accepted for publication 15/4/2020.

ABSTRACT

In recent years, the period of traditional CMOS, it may be possible to continue functional scaling by integrating alternative electronic devices) onto a silicon platform . These alternative electronic devices include resonant tunneling diode, single electron transistor, molecular field effect transistor, carbon nanotube field effect transistor, spin field effect transistor (spin FET), and graphene field effect transistor (graphene FET). We have developed NEMO-VN2-2019, a quantum device modeling tool that simulates emerging nanoelectronic devices. These devices include the resonant tunneling diode, the single electron transistor, the molecular field effect transistor, the carbon nanotube field effect transistor, spin field effect transistor, graphene field effect transistor. The non-equilibrium Green's function method is used to perform a comprehensive study of emerging nanoelectronic devices. The program has been written by using graphic user interface of Matlab. NEMO-VN2-2019 uses Matlab to solve the Schrodinger equation to get current-voltage characteristics of quantum devices. In this work, we provide a short overview of the theoretical methodology using non-equilibrium Green's function method for modeling of the nanoscale devices, their simulations and updated information of NEMO-VN2-2019.

Keywords: resonant tunneling diode; single electron transistor; molecular field effect transistor; carbon nanotube field effect transistor; spin field effect transistor; graphene field effect transistor; current-voltage characteristics.

1. INTRODUCTION

The dimensional scaling of CMOS device and process technology will become much more difficult as the semiconductor industry approaches 10 nm (6 nm physical channel length) around year 2019 and will eventually approach asymptotic end according to the International Technology Roadmap for Semiconductor for emerging research devices [1]. Beyond this period of traditional CMOS(,) it may be possible to continue functional scaling by integrating alternative electronic devices onto a silicon platform. These alternative electronic devices include resonant tunneling diode, single electron transistor, molecular field effect transistor, carbon nanotube field effect transistor, spin field effect transistor (spin

FET), and graphene field effect transistor (graphene FET).

In recent years, a vigorous research effort to demonstrate spin transistors has been pursued. One of the motivations has been that spin transistors are identified as one of the most promising alternatives to traditional MOSFET by the International Technology Roadmap for Semiconductors [1]. Simulations have predicted that spin transistors can scale in their size with smaller switching energy and less overall power dissipation than that of MOSFET. The idea of spin field-effect transistor sparked after Fert et al. [2] and Grunberg et al. [3] discovered the giant magneto-resistance effect in magnetic multilayer systems in 1988. They found huge differences in current coming out of a magnetic and metallic multilayer system

when the magnetic layers had the same or different scattering of electrons. Following the preliminary realization of the potential benefits of utilizing spin property, Datta and Das proposed an electron wave analog of the electro-optic light modulator in the late 1989 [4]. Most of the today's interest in this newly born field of study is motivated by their well-known proposed device which is now known as spin field-effect transistor (spin FET).

Graphene [5-7] has been one of the most rigorously studied research materials since its inception in 2004. There has been a lot of study focused on transport properties of graphene. Many issues related to transport properties of graphene field-effect transistors. Experimental [8-11] and theoretical [12-14] studies have shown that even though being a gapless semi-metallic material, a graphene FET shows saturate current-voltage behaviors. In previous studies [12-14], to describe semi-classical transport of graphene FET at a channel length that a semi-classical Boltzmann transport equation (BTE) is solved self consistently with Poisson's equation. Monte-Carlo method and numerical solutions of solving BTE have been implemented, they are limited to two-dimensional k-space, which assumes a homogeneous material and therefore it has limitations to describe transport properties in the graphene transistor accurately.

This paper reviews the capabilities of the NEMO-VN2-2019, summarizes the theoretical approach, updates two types of nanotransistors including SpinFET and GNR-FET, and gives typical examples of simulations of the software program.

2. QUANTUM DEVICES AND SIMULATION METHOD

2.1 Non-equilibrium Green's function method in modeling of quantum devices

The NEGF model of the quantum device used for transport simulations is shown in figure 1.

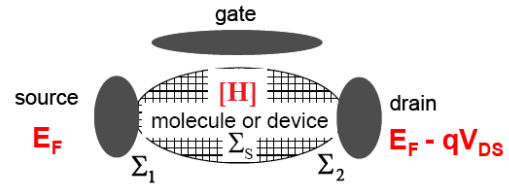


Figure 1. The model of the quantum device.

Here, H is the device Hamiltonian, and the self-energy functions $\Sigma_{1,2}$ present the semi-infinite ideal source-drain contacts. Σ_S is the self-energy for the e-ph interaction, and one sets $\Sigma_S = 0$ for the ballistic approximation.

The current flows from source to drain can be defined [15]

$$I = \frac{4e}{\hbar} \int_{-\infty}^{+\infty} \frac{dE}{2\pi} T(E) [f(E - E_S^F) - f(E - E_D^F)] \quad (1)$$

where $f(E)$ is the Fermi distribution, and $E_{S/D}^F$ denotes the source and drain Fermi energies, respectively. With the transmission coefficient $T(E)$ given by

$$T(E) = \text{Trace} [\Gamma S(E) G(E) \Gamma D G^+(E)] \quad (2)$$

where level broadening can be defined as follows:

$$\Gamma(E) = i[\Sigma(E) - \Sigma^+(E)] \quad (3)$$

where $\Sigma^+(E)$ represents the Hermitian conjugate of Σ matrix defined by (5).

The retarded Green's function for the device in matrix form is given by

$$G(E) = [(E + i\eta^+)I - H - \Sigma(E)]^{-1} \quad (4)$$

where η^+ is an infinitesimal positive value, and I is the identity matrix.

The self-energy contains contributions from all mechanisms of relaxation, which are the source and drain electrodes, and from scattering

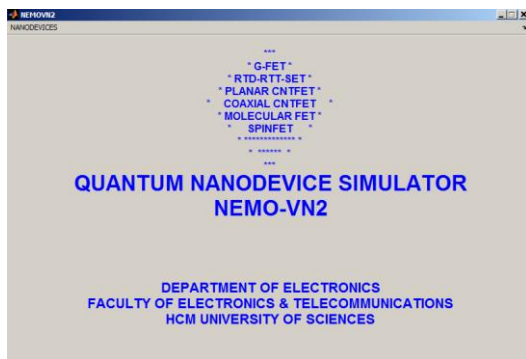
$$\Sigma(E) = \Sigma_1(E) + \Sigma_2(E) + \Sigma_S(E) \quad (5)$$

Note that, in (5), the self-energy functions are, in general, energy dependent.

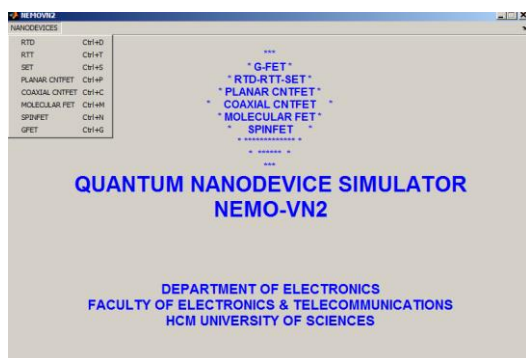
2.2 Simulation results and discussion

NEMO-VN2 2019 has a rich variety of nano-device models, while it provides the

maximum flexibility in term of applicability to types of different devices and test conditions. The problem is that NEMO-VN2-2019 requires over 100 simulation parameters. Traditional device simulation programs force the users to familiarize themselves with all available simulation parameters and ensure that they are set correctly. To minimize this burden for the users, NEMO-VN2-2019 uses a hierarchical approach to input and displays simulation parameter values. The top level of this hierarchy specifies the highest level option (nanodevices). Subsequent levels contain more detailed options such as current-voltage characteristics of devices, types of material, size of devices, temperature, colors, etc.



(a)



(b)

Figure 2. a) The NEMO-VN2-2019 main screen, b) Pressing the left mouse pointer on “NANODEVICES”, it displays a list of simulated nano-devices.

The main screen shown in figure 2a is the central location where the user controls the NEMO-VN2-2019 simulation program. From main screen, the user can choose various types of nano-device simulations by clicking the left

mouse pointer on sub-menu of nanodevices (in the left top corner). In this manner, the user can quickly enter the device list and hot keys with minimum of typing. Clicking the left mouse pointer on each item in the device list or using hot keys initiates the selection of models which is used to calculate the current - voltage characteristics (figure 2b)

Resonant Tunneling Devices

Resonant tunneling diodes (RTDs) are two terminal devices that have a very high switching speed and exhibit a region of negative differential resistance in their I-V curves. These two characteristics make them potentially attractive as high-speed switching devices.

Current-voltage characteristics and model of the RTD are shown in figure 3. Characteristic curve is divided into two parts: positive and negative resistances. Here, it should be emphasized that the peak current and the valley current of the RTD are perfectly represented by the model.

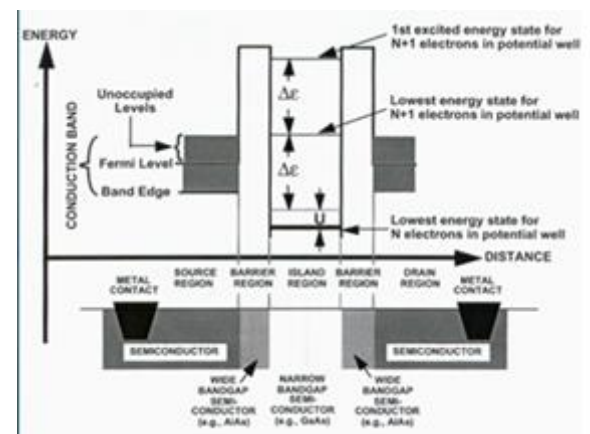
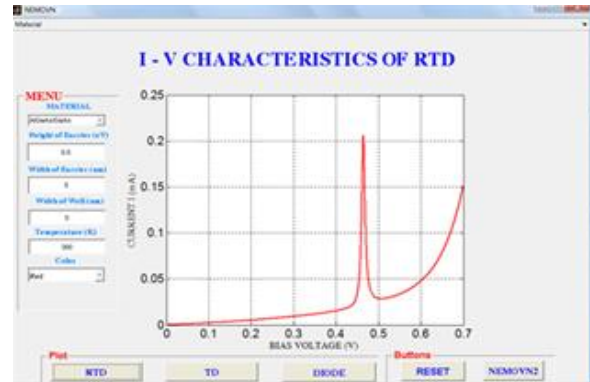


Figure 3. Current-voltage characteristics of RTD at room temperature.

Single Electron Transistor

A model of single electron transistor (SET) called a capacitance model is shown in figure 4. A SET is made from two tunnel junctions that share a common electrode. A tunnel junction consists of two pieces of metal supported by a very thin (about 1 nm) insulator (Figure 4a). The only way for electrons is from one of the metal electrodes to travel to the other electrode is to tunnel through the insulator. Since tunneling is a discrete process, the electric charge that flows through the tunnel junction in multiples of e , the charge of electron.

A quantum dot (QD) is usually formed in two dimensional electron gas (2DEG) in GaAs/AlGaAs using standard electron beam lithography. The quantum dot is connected to the source and drain electrodes through tunnel barriers. The potential in the dot can be controlled by the gate electrode which is capacitively coupled to the quantum dot (figure 4b). The current through the quantum dot can be periodically modulated by the gate voltage ($V_G = (2n+1)e/2CG$, Coulomb oscillations). When the current is zero (Coulomb blockade, CB), the number of electrons is fixed. Therefore, it differs exactly by one on both sides of the current peak.

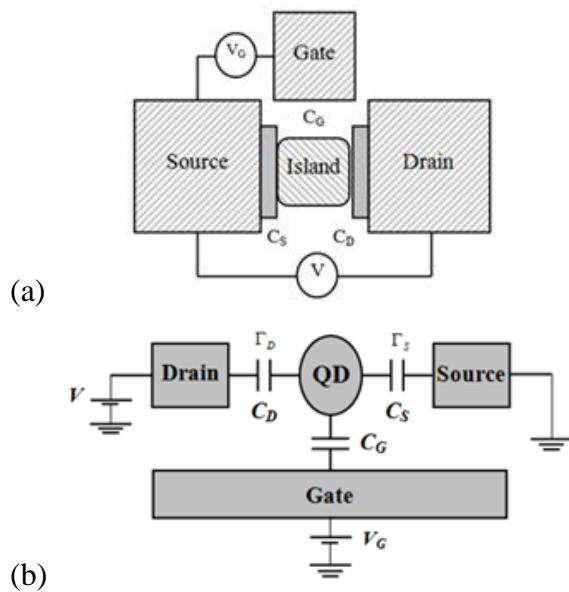


Figure 4. a) Structure of single electron transistor; b) equivalent schematic diagram of SET.

By utilizing NEMO-VN2-2019, the I_D - V_G characteristics of SET having the given parameters are shown in figure 5.

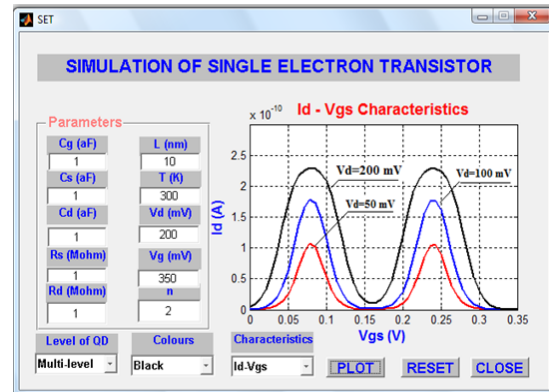


Figure 5. Typical I_D - V_G characteristics (Coulomb oscillations) of SET.

Molecular Field Effect Transistor

Molecular field effect transistor (MFET) is a promising alternative candidate of traditional MOSFET in future due to its small size, low power and high speed. The structure of the MFET is in shape like traditional MOSFET, but its conductive channel is replaced by a benzene-1,4-dithiolate molecule.

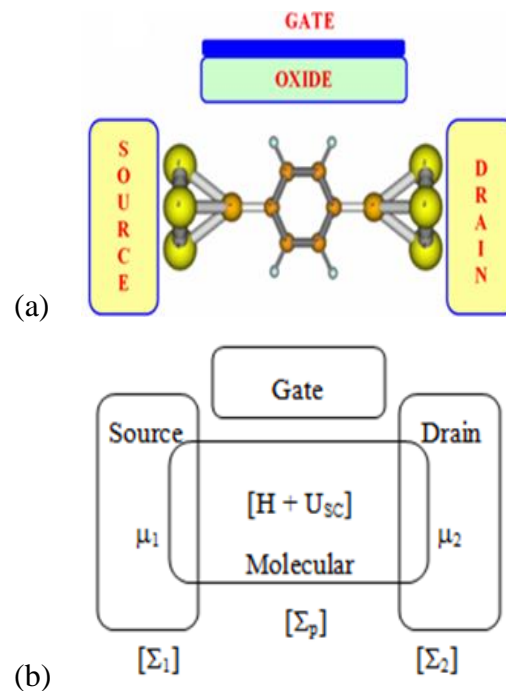
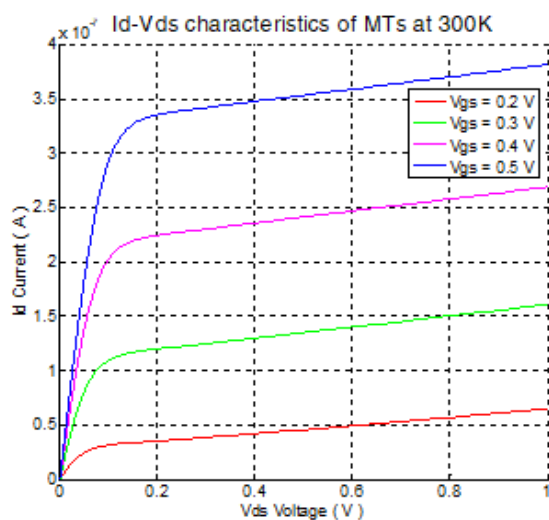


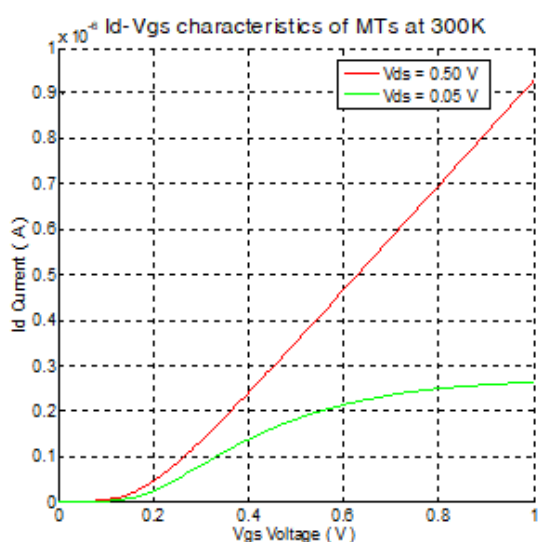
Figure 6. a) Schematic view of a molecule coupled to source and drain contacts. b) The molecule is described by a Hamiltonian H and a self-consistent potential USC .

A schematic view of a molecule coupled to gold source (S) and drain (D) contacts is shown in figure 6. As an example, we use the benzene-1,4-dithiol molecule which consists of a phenyl ring with thiol(-SH) end groups. A gate terminal may be used to modulate the conductance of the molecule. The coupling between the gate and the molecule is purely capacitive – there is no gate current.

Current–voltage characteristics of the molecular field effect transistor at different values of bias voltage are shown in figure 7.



(a)



(b)

Figure 7. Current–voltage characteristics of the MFET: (a) $I_D = f(V_D)$ for different values of the gate voltages and (b) $I_D = f(V_G)$ for different values of the drain voltages.

The ID-VD characteristics of the MFET are shown in figure 7a. ID-VD curves are divided into three regions: linear, non-linear and saturate. When drain voltage, VD is small, the drain current, ID is linearly increased. When the drain voltage, VD is great enough, the drain current is changed little.

The ID-VG characteristics of the MFET are shown in figure 7b. The ID-VG curves are exponential functions in shape.

Carbon Nanotube Field Effect Transistor

Carbon nanotube field effect transistor (CNTFET) is a three-terminal device consisting of a semiconducting nanotube bringing two contacts (source and drain), and acting as a carrier channel, which is turned ON or OFF electrically via the third contact (gate). Presently, there are several types of CNTFETs have been fabricated, but CNTFET geometries may be grouped in two major categories: planar and coaxial CNTFETs, whether planar or coaxial, relies on simple principles, while being governed by additional phenomena such as 1D density of states (DOS), ballistic transport, and phonon scattering.

Planar CNTFETs (Figure 8a) constitute the majority of devices fabricated to date, mostly due to their relative simplicity and moderate compatibility with existing manufacturing technologies. The coaxial geometry (Figure 8b) maximizes the capacitive coupling between the gate electrode and the nanotube surface, thereby inducing more channel charge at a given bias than other geometries. This improved coupling is desirable in mitigating the short-channel effects that plague technologies like CMOS as they downside device features. The key device dimensions are: the gate inner radius, R_g , and thickness, t_g ; the nanotube radius, R_t , and length L_t ; the insulator thickness $t_{ins} = R_g - R_t$; the end-contact radius, r_c (the source and drain may sometimes be of different sizes), and length, L_c ; and the gate under lap L_u .

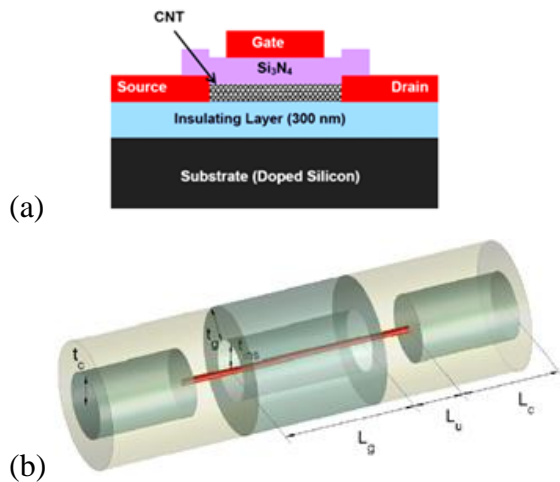


Figure 8. Structures of CNTFETs: a) planar, b) coaxial.

Figure 9 compares the ID-VD results for two types of planar and coaxial CNTFETs having the length of 20 nm under ballistic transport and that with phonon scattering.

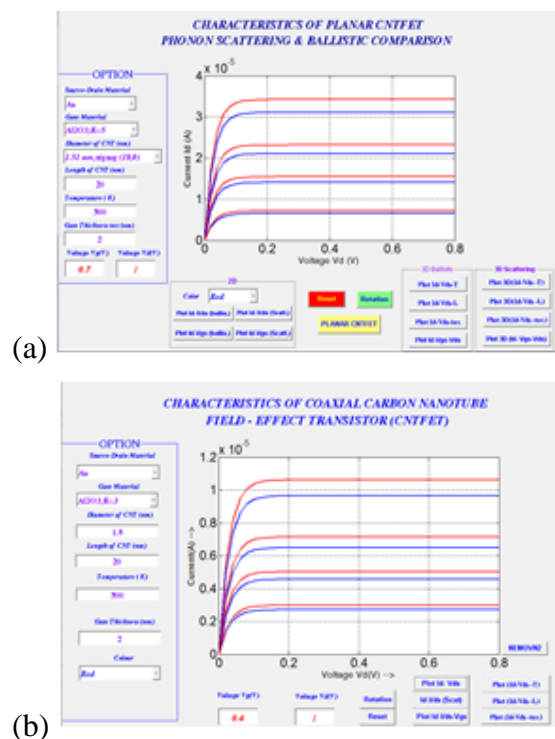


Figure 9. ID-VD characteristics of a) planar and b) coaxial CNTFETs having the length of 20 nm under ballistic transport (red color), with scattering (green color).

It is shown that scattering can have an appreciable effect on the on-current. At $V_G = 0.7$ V, in the planar and coaxial CNTFETs, the on-current is reduced by 9% due to the

phonon scattering. It can be noted that when the gate voltage is increased, the saturate drain current gradually increased.

Datta and Das Spin Field Effect Transistor

In the late 1989, Supriyo Datta and Biswajit Das from Purdue University proposed an electron wave analog of the electro-optic light modulator. Most of the today's interest in spintronics is motivated by their well-known proposed device which is known as the spin field-effect transistor.

Datta-Das's paper spurs a new research direction. The operation of ideal Datta-Das spin FET can be sketched in figure 10.

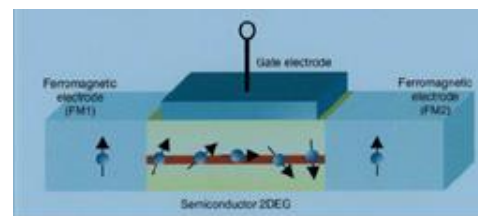


Figure 10. Basic configuration of a spin field-effect transistor proposed by Datta and Das.

Using “menu” of the main screen we can choose materials, temperature, gate thickness, gate length for simulation of ID-VD characteristics of spin FET. Five semiconductors such as GaAs, Si, InAs, InSb, $Hg_{0.775}Cd_{0.225}Te$ can be chosen for constructing channel of spin FET by using menu. ID-VD curves can be divided into three regions: linear, non-linear and saturate. ID starts from zero and increases linearly when drain voltage, V_D is small. ID is not changed when V_D is greater than $(V_G - V_{th})$, where V_{th} is threshold voltage.

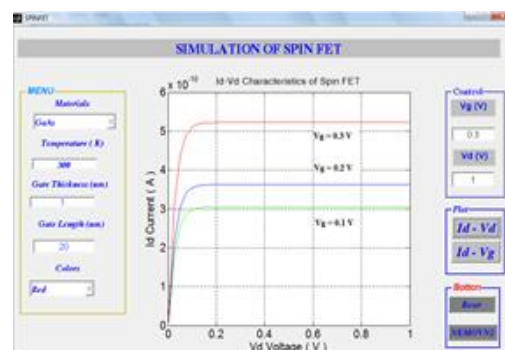


Figure 11. Typical ID-VD characteristics of spin FET simulated by NEMO-VN2-2019.

Top-gate Graphene field effect transistor

Graphene FET is a three-terminal device consisting of a semiconducting graphene connecting two contacts (source and drain), and acting as a carrier channel, which is turned ON or OFF electrically via the third contact (gate). Top-gate graphene FET as shown in Figure 12 is simulated. The normal device has a top-gate insulator of Al₂O₃ [16].



Figure 12. Structure of top gated graphene field-effect transistor [16] is used in our simulations.

We start by simulating ID-VD characteristics of top-gated graphene FET. Figure 12 shows the schematic view of the device used in our simulations. Top-gate graphene FET with two-dimensional graphene as the channel is simulated. The device is simulated with Al₂O₃ as the dielectric material which has been predicted to be one of the promising dielectric material for graphene FETs in recent experiment [16]. All the simulations have been done for channel length of the graphene FET, L = 10 nm.

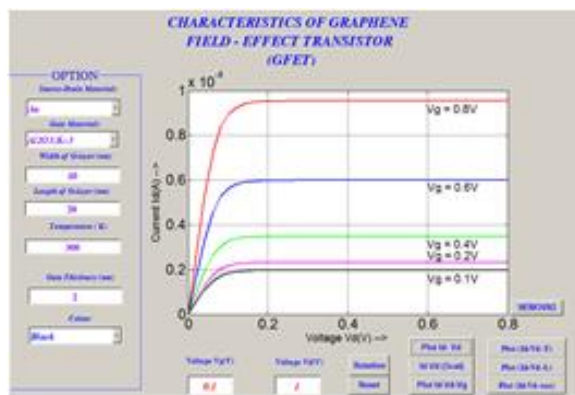


Figure 13. The ID-VD characteristics of the top-gate graphene field effect transistor at different gate voltages, VG = 0.1 V, 0.2 V, 0.4 V, 0.6 V, 0.8 V.

Figure 13 shows the ID-VD characteristics of the graphene FET having the length of 20 nm at different gate voltage, VG = 0.1 V, 0.2 V, 0.4 V, 0.6 V, and 0.8 V. It can be noted that due to semiconductor graphene used in channel of the top-gate graphene FET, ID-VD curves are divided into three regions: linear, non-linear and saturate. When drain voltage is small, the drain current is linearly increased. When the drain voltage is great enough, the drain current is mostly not changed.

Figure 14 shows the ID-VD characteristics of the top-gate GNR-FET having the length of 10 nm under ballistic transport and that with phonon scattering. It is shown that scattering can have an appreciable effect on the ON-current. At VGS = 0.8 V, the ON-current is reduced by 9% due to the phonon scattering.

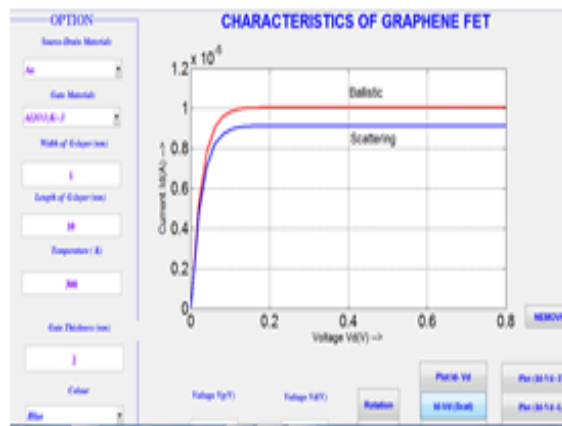


Figure 14. The ID-VD characteristics of the top-gate GNR-FET at VG = 0.8 V for ballistic, scattering, where the length of the gate is LG=10 nm.

3. CONCLUSION

We present briefly here the description of the NEMO-VN2-2019. The NEGF method is used to simulate transport of carriers in all nano-devices including the resonant tunneling diode, the single electron transistor, the molecular field effect transistor, the planar and coaxial CNTFETs and update the spin FET, the top-gate graphene FET. We also demonstrate the abilities of the NEMO-VN2-2019 for simulating nano-devices using GUI in Matlab. Finally, we display some

typical simulation results obtained by this method, such as the current-voltage characteristics of the nano-devices. NEMO-VN2-2019 is usefully utilized not only for modeling and simulation of devices in nano-scale, but also for training graduated students on Nano electronics.

REFERENCES

- [1] The international Technology Roadmap for Semiconductor, 2005 Edition.
- [2] M. N. Baibich, J. M. Broto, A. Fert, F. Nguyen Van Dau, F. Petroff, P. Etienne, G. Creuzet, A. Frederic, and J. Chazelas, Giant magneto resistance of (001)Fe/(001)Cr magnetic super lattices, *Physical Review Letters* 61 (1988), 2472-2475.
- [3] G. Binash, P. Grunberg, F. Saurenbach, and W. Zinn, Enhanced magneto resistance in layered magnetic structures with anti-ferromagnetic interlayer exchange, *Phys. Rev. B* 39 (1989) 4828-4830.
- [4] S. Datta and B. Das, Electronic analog of the electro-optic modulator, *Appl. Phys. Lett.*, 56 (1990) 665-667.
- [5] K.S Novoselov, A.K. Giem, S.V. Morozov, D. Jang, Y. Zhang, S.V. Dubonos, I.V. Grigorieva, and A.A. Firsov, Electric field effect in atomically thin films, *Science* 306, No.5696, (2004) 666-669.
- [6] L. Jiao, L. Zhang, X. Wang, G. Diankov, and H. Dai, Narrow graphene Nano ribbons from carbon nanotubes, *Nature* 458 (2009) 877-880.
- [7] X. Li, X. Wang, L. Zhang, S. Lee, H. Dai, Chemically drive, ultra smooth graphene Nano ribbon semiconductors, *Science* 319, No. 5867 (2008) 1229-1232.
- [8] I Meric, M.Y. Han, A.F. Young, B. Oezylmaz, P. Kim, and K. Shepard, Current saturation in zero-band gap top-gated graphene field-effect transistors, *Nat. Nanotech* 3 (2008) 654-659.
- [9] I. Meric, C. Dean, A.F. Young, J. Hone, P. Kim, and K. Shepard, Graphene field-effect transistors based on boron nitride gate dielectrics, *IEDM Tech. Dig.* (2010) 556-559.
- [10] M. Freitag, M. Steiner, Y. Martin, V. Perebeinos, Z. Chen, J.C. Tsang, and P. Avouris, Energy dissipation in graphene field effect transistors, *Nano Lett.*, 9, No.5 (2009) 1883-1888.
- [11] V.E. Dorgan, M.H. Bae, E. Pop, Mobility and saturation velocity in graphene on SiO₂, *Appl. Phys. Lett.* 97, No.8 (2010) 082112/1-3.
- [12] A.M. Dasilva, R. Zou, J.K. Jain, and J. Zhu, Mechanism for current saturation and energy dissipation in graphene transistors, *Phys. Rev. Lett.* 104, No.24 (2010) 236601-236604.
- [13] J. Chauhan and J. Guo, High-field transport and velocity saturation in graphene, *Appl. Phys. Lett.* 95 (2009) 023120/1-3.
- [14] R.S. Shishin and D.K. Ferry, Velocity saturation in intrinsic graphene, *J. Phys. Condense. Matter* 21 (2009) 344201.
- [15] S. Datta, *Quantum Transport: Atom to Transistor*, Cambridge University Press, (2005).
- [16] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tuctuc, and S.K. Banerjee, Realization of a high mobility dual-gated graphene FET with Al₂O₃ dielectric, *Appl. Phys. Lett.* 94 (2009) 062107/1-3

Corresponding author:

Le Hoang Minh

Ho Chi Minh City University of Technology and Education

Email: minhhlh@hcmute.edu.vn