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Quasi Z-Source Neutral-Point-Clamped Inverter Using SVM Technique to Eliminate Common Mode Voltage

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ABSTRACT

In recent year, common mode voltage (CMV) elimination methods are considered to improve the reliability of three-level quasi-switched boost T-type inverter (TL-qSBT^{2}I). The space-vector modulation method (SVM) can control the inverter operation to eliminate the CMV. The proposed method applies medium vectors and zero vector to synthesize the reference vector to eliminate CMV while the output voltage is unchanged compared to SinPWM technique. In order to prevent the active vectors and the output voltage from being affected, the shoot-through vector is inserted inside the zero vector. Accordingly, the proposed method not only maintains the CMV elimination advantage of the SVM technique for TL-qSBT^{2}I but also reduces the inductor current ripple and enhances the voltage gain without any topology modification or adding electrical components. Results from simulations and experiments are used to evaluate the efficiency of the suggested strategy. Additionally, by comparing the proposed scheme with the traditional pulse-width modulation technique, the superiority of the proposed scheme is shown.

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1. Introduction

Nowadays, a variety of applications, including uninterrupted power supply (UPS), photovoltaic (PV) systems, wind power, hybrid electric vehicles (HEV), etc., use multiple voltage source inverters (VSI). [1]-[3]. Traditional VSI topologies, on the other hand, operate like buck converters and provide peak-to-peak output voltages that are lower than the DC-link voltage [4]. The Z-source (ZS) network was investigated in [5] in order to get around these restrictions. This new topology, which has buck-boost voltage capability and ST immunity, is known as a single-stage inverter and requires the use of one additional diode, two extra inductors, and two extra capacitors. The combination of the ZS network and the traditional three-level NPC inverter was investigated in the literature [6]. In order to overcome the limitations of ZS networks, the work [1], [7] presented a novel type of impedance network termed quasi-Z-source (qZS). The output terminal of these investigations generated a three-level voltage by cascading two identical qZS networks. As a result, it enhances the output voltage quality. However, it also results in more inductors and capacitors, which are passive parts. As a result, the system's weight, size, and price all considerably increase. The quasi-switched boost (qSB) network saves one inductor and one capacitor as compared to the qZS design while maintaining the boost factor by adding two additional active switch [8]. In order to improve the ripple in the inductor current and increase the converter's boost factor, the report [9] suggested a pulse with modulation (PWM) technique based on the phase shift carrier approach. A three-level Neutral-Point-Clamped inverter (TL-NPCI) and qSB network combination has been addressed in the literature [10]. In this study, a three-level voltage at the output voltage was produced by cascading two identical qSB networks together with one fewer inductor. Additionally, a PWM technique to improve the converter's boost factor and decrease inductor current ripple was described .

The common-mode voltage (CMV), which the inverter produces while it is operating, can lead to a variety of issues, including bearing currents, shaft voltage in applications using motor drives, and electromagnetic interference [11]. As a result, it will shorten the inductor motor's lifetime or have an

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bearing on other electronic devices that are local to the inverter. Next, the switching sequence is changed to add the ST state, which ensures the boost capability. Meanwhile, the CMV magnitude is kept and applied to the qZS inverter [12]. This technique do not, however, totally get rid of CMV.

The quasi Z-Source (qZS) network and the traditional three-level neutral point clamped inverter (NPCI) are combined in this paper. It is suggested to use the SVM approach to get the elimination of CMV for TL-qZSNPCI. In this method, a reference vector is synthesized by using medium vectors and a zero vector. As a result, CMV is eliminated. Results from simulations and experiments are used to evaluate the efficiency of the suggested strategy. Additionally, by comparing the proposed scheme with the traditional pulse-width modulation technique, the superiority of the proposed scheme is shown.

2. Three-level quasi Z-source NPC inverter topology

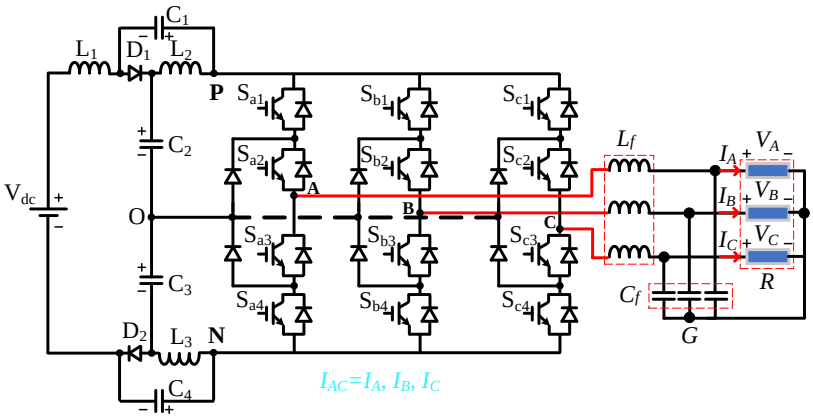

Figure 1. *Three-level quasi Z-source NPC inverter*

2.1. Three-level quasi-switched boost NPC inverter topology

As illustrated in Fig. 1, the introduced topology consists of the MqSB network which is formed by two identical impedance networks including two inductors (L_1, L_2), two capacitors (C_1, C_2), four diodes (D_1, D_2, D_3, D_4), two active switches (T_1, T_2) and the traditional NPC structure.

2.1.1. Operation principles

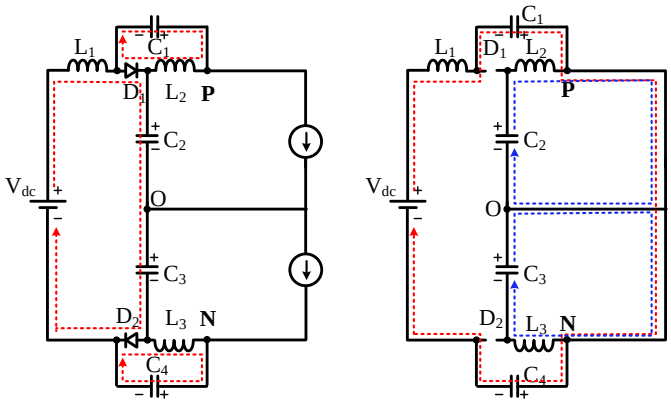

Figure 2. *Operating states of the three-level qZSNPCI. (a) NST mode, (b) ST mode.*

Similar to other single-stage inverters, this structure also operates under two main modes: non-shoot-through (NST) mode and shoot-through (ST) mode. In NST mode, the inverter is able to produce three-level voltage at the output terminal by triggering corresponding switches. To simply, in non-ST modes, the inverter side is considered as a current source, I_{AC} as shown in Table I. When S_{X1} and S_{X2} are switched "ON", the output of the inverter is achieved $+V_{PN}/2$, where V_{PN} is the DC-link voltage generated by the MqSB network. While the output voltage obtains $-V_{PN}/2$ when S_{X3} and S_{X4} are turned "ON". The zero value is produced at output voltage when S_{X2} and S_{X3} are triggered "ON". The NST mode consists of two sub-mode which are NST mode 1 and NST mode 2, as presented in Table I. The ST mode is

achieved when all switches of inverter leg are triggered "ON", simultaneously. As a result, the output load voltage in this time interval is zero. Therefore, the ST state is generated in the zero vector in order not to cause the distortion at output voltage.

Table 1. *Switching states of the proposed inverter (x=a, b, c)*

Mode	Triggered Switches	ON Diodes	V_X
NST	S_{X1}, S_{X2}	D_1, D_2, D_3, D_4	$+V_{PN}/2$
	S_{X2}, S_{X3}		0
	S_{X3}, S_{X4}		$-V_{PN}/2$
ST	S_{X1}, S_{X2}, S_{X3}, S_{X4}	D_1, D_4	0

2.1.1.1. NST mode

Considering the non-short circuit state as shown in Figure 2.7(a), the diodes D_1 and D_2 are forward biased, the two capacitors C_2 and C_3 are stored energy from the input power V_{dc} and the voltage of the inductor L_1. Meanwhile, capacitors C_1 and C_4 store energy from inductor L_2 and L_3. The duration of this state is $(1\text{-}D_{ST}).T$. The voltage across inductors L_1, L_2, and L_3 are obtained as following equations:

$$\begin{cases} V_{PN} = V_{L1} + V_{C2} + V_{C3} \\ V_{L2} = -V_{C1} \\ V_{L3} = -V_{C4} \end{cases} \quad (1)$$

2.1.1.2. ST mode

Considering the ST mode as shown in Figure 2.7(b) the switches of the inverter (S_{1x}, S_{2x}, S_{3x}, and S_{4x}) are turned on at the same time, making diodes D_1 and D_2 reverse biased, meanwhile, the input power supply V_{dc} and the two capacitors C_2 and C_3 provide power to the two inductors L_2 and L_3, the input power V_{dc} and the two capacitors C_1 and C_4 supply power to inductor L_1. The duration of the ST mode is $D_{ST}.T$. The voltage across inductors L_1, L_2, and L_3 are obtained as following equations:

$$\begin{cases} V_{PN} = V_{L1} - V_{C1} - V_{C4} \\ V_{L2} = V_{C2} \\ V_{L3} = V_{C3} \end{cases} \quad (2)$$

2.1.2. Steady-State Analysis for the TL-qZSNPCI

Applying the volt-second balance for inductors to (1) and (2) with the ST time in one carrier cycle being $D_{ST}.T$ and the NST time being $(1\text{-}D_{ST}).T$, The voltage across the capacitors can be calculated as follows:

$$\begin{cases} V_{C1} = V_{C4} = \dfrac{V_{dc.}(1 - D_{ST})}{2.(1 - D_{ST})} \\ V_{C2} = V_{C3} = \dfrac{V_{dc.}D_{ST}}{2.(1 - D_{ST})} \end{cases} \quad (3)$$

The peak value of DC-link voltage (V_{PN}) is identified as:

$$V_{PN} = V_{dc}.\frac{1}{1 - 2D_{ST}} \quad (4)$$

The peak value of output phase voltage is identified as:

$$V_{x,peak} = m\frac{2}{\sqrt{3}}\frac{V_{PN}}{2} = \frac{m}{\sqrt{3}}.\frac{1}{1 - 2D_{ST}}V_{dc} \quad (5)$$

The boost factor of inverter is calculated as:

$$B = \frac{V_{PN}}{V_{dc}} = \frac{1}{1 - 2D_{ST}} \quad (6)$$

where,

V_{C1}, V_{C2}, V_{C3}, V_{C4} - capacitor voltage of C_1, C_2, C_3, and C_4;

V_{dc} - input DC voltage of the inverter;

D_{ST} - ST duty ratio.

2.2. The Proposed SVM Scheme for TL-qZSNPCI-ECMV

Table 2. *Common-mode voltage (CMV) value of the TL-qZSNPCI-ECMV*

Mode	T_A	T_B	T_C	CMV	Mode	T_A	T_B	T_C	CMV
1	-1	-1	-1	$-V_{PN/2}$	14	**0**	**0**	**0**	**0**
2	-1	-1	0	$-V_{PN/3}$	15	0	0	1	$V_{PN/6}$
3	-1	-1	1	$-V_{PN/6}$	16	**0**	**1**	**-1**	**0**
4	-1	0	-1	$-V_{PN/3}$	17	0	1	0	$V_{PN/6}$
5	-1	0	0	$-V_{PN/6}$	18	0	1	1	$V_{PN/3}$
6	**-1**	**0**	**1**	**0**	19	1	-1	-1	$-V_{PN/6}$
7	-1	1	-1	$-V_{PN/6}$	20	**1**	**-1**	**0**	**0**
8	**-1**	**1**	**0**	**0**	21	1	-1	1	$V_{PN/6}$
9	-1	1	1	$+V_{PN/6}$	22	**1**	**0**	**-1**	**0**
10	0	-1	-1	$-V_{PN/3}$	23	1	0	0	$V_{PN/6}$
11	0	-1	0	$-V_{PN/6}$	24	1	0	1	$V_{PN/3}$
12	**0**	**-1**	**1**	**0**	25	1	1	-1	$V_{PN/6}$
13	0	0	-1	$-V_{PN/6}$	26	1	1	0	$V_{PN/3}$
					27	1	1	1	$V_{PN/2}$

During operation, the MLIs generate CMV, which is identified as the voltage between load neutral point "G" and DC-link neutral point "O". It can be calculated through three-phase output voltage and the CMV, as presented in (7).

$$V_{GO} = \frac{V_{AO} + V_{BO} + V_{CO}}{3} = \frac{T_A + T_B + T_C}{6}.V_{PN} \quad (7)$$

where V_{AO}, V_{BO}, and V_{CO} are three-phase output pole voltages.

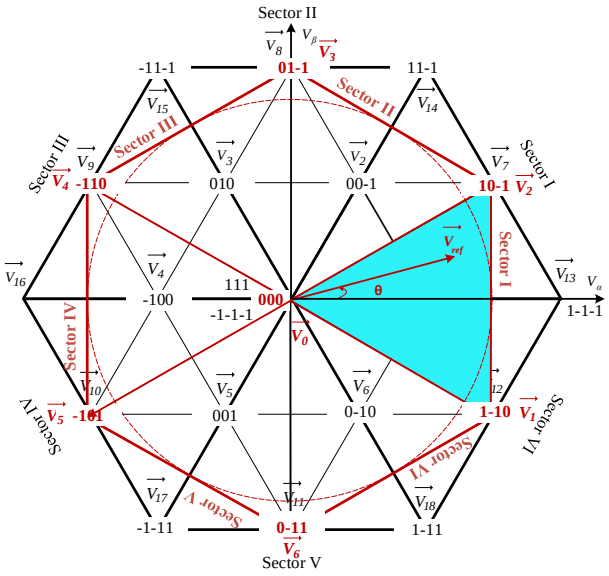

Figure 3. *Space vector diagram of the proposed strategy.*

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Based on equation (7), for each vector [T_A T_B T_C], a CMV value is always determined. Table 2 lists the CMV values corresponding to the vectors of the TL-qZSNPCI.

Table 2 shows that the medium vectors (-101; -110; 0-11, 01-1, 1-10 and 10-1) and the zero vector [OOO] produce the smallest CMV, while the large vectors produce CMV with amplitudes ranging from -$V_{PN/6}$ to +$V_{PN/6}$. The small vectors produce different CMV values, the largest being $V_{PN/3}$, while the zero vectors [111] and [-1-1-1] produce the CMV with the largest amplitude, $V_{PN/2}$.

It can be seen that the state vectors of TL-NPCI generating CMV with value 0V (see table 2) are vectors $[T_a, T_b, T_c]$ satisfying the condition:

$$T_a + T_b + T_c = 0 \tag{8}$$

Then, the vector diagram for the CMV elimination algorithm using 7 vectors divided into 6 sectors is shown in Figure 3.

Assume $\overrightarrow{V_{ref}}$ is located in sector I, region 1 as depicted in Figure 3.

Then, $\overrightarrow{V_{ref}}$ is synthesized by vectors $\overrightarrow{V_0}, \overrightarrow{V_1}, \overrightarrow{V_2}$ with the relationship presented through the following equation:

$$\overrightarrow{V_{ref}}.T = \overrightarrow{V_0}.T_0 + \overrightarrow{V_1}.T_1 + \overrightarrow{V_2}.T_2 \tag{9}$$

Where T is the carrier period and T_0, T_1, T_2 is the on-times of the vectors $\overrightarrow{V_0}, \overrightarrow{V_1}, \overrightarrow{V_2}$ in one carrier period. The relationship between T_0, T_1, T_2 and T is represented by the equation:

$$T_0 + T_1 + T_2 = T \tag{10}$$

The vectors $\overrightarrow{V_{ref}}, \overrightarrow{V_0}, \overrightarrow{V_1}, \overrightarrow{V_2}$ are determined through the expression (11)

$$\begin{cases} \overrightarrow{V_{ref}} = m.\dfrac{V_{dc\_link}}{2}.e^{j\varphi} \\ \overrightarrow{V_0} = 0 \\ \overrightarrow{V_1} = m.\dfrac{\sqrt{3}V_{dc\_link}}{3}.e^{-j\frac{\pi}{6}} \\ \overrightarrow{V_2} = m.\dfrac{\sqrt{3}V_{dc\_link}}{3}.e^{j\frac{\pi}{6}} \end{cases} \tag{11}$$

From equations (9), (10), and (11), it is possible to determine the lifetime of the vectors $\overrightarrow{V_0}, \overrightarrow{V_1}, \overrightarrow{V_2}$ as follows:

$$\begin{cases} T_0 = T - t_1 - t_2 \\ T_1 = T.m.\sin\left(\dfrac{\pi}{6} - \varphi\right) \\ T_2 = T.m.\sin\left(\dfrac{\pi}{6} + \varphi\right) \end{cases} \tag{12}$$

Table 3. *CMV elimination vector sequence*

Sector	Propose sequence
I	[000]- [10-1]-[1-10]-[1-10]-[10-1]-[000]
II	[000]-[01-1]-[10-1]-[10-1]-[01-1]-[000]
III	[000]-[-110]-[01-1]-[01-1]-[-110]-[000]
IV	[000]-[-101]-[-110]-[-110]-[-101]-[000]
V	[000]-[0-11]-[-101]-[-101]-[0-11]-[000]
VI	[000]-[1-10]-[0-11]-[0-11]-[1-10]-[000]

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The Vectors are arranged in switching order as shown in Figure 4(a). The vector sequence for the remaining sectors can be determined from Table 3.

To ensure the boost for the TL-qZSNPCI configuration without distortion of the output voltage. The order of vectors in the case $\overrightarrow{V_{ref}}$ is rearranged as shown in Figure 4(b). The vector sequence for the remaining sectors can be represented through Table 4.

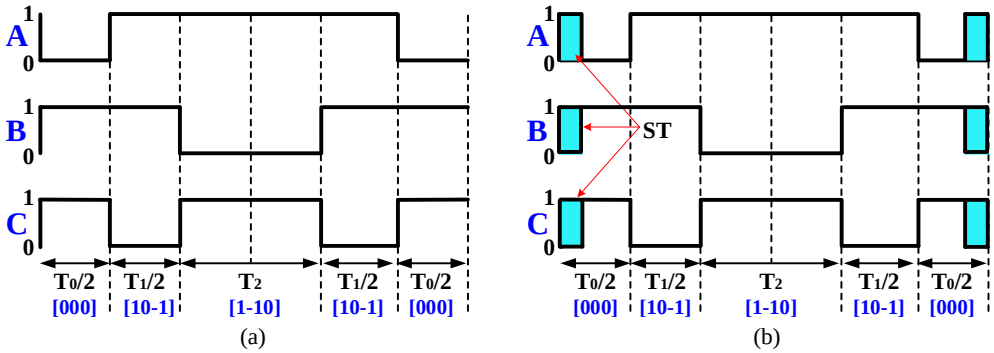


Figure 4. *Vector sequence for sector I according to the traditional method.*

Table 4. *proposed CMV elimination vector sequence*

Sector	proposed pulse sequence after ST pulse insertion
I	[000]-[FFF]-[10-1]-[1-10]-[1-10]-[10-1]-[FFF]-[000]
II	[000]-[FFF]-[01-1]-[10-1]-[10-1]-[01-1]-[FFF] [000]
III	[000]-[FFF]-[-110]-[01-1]-[01-1]-[-110]-[FFF]-[000]
IV	[000]-[FFF]-[-101]-[-110]-[-110]-[-101]-[FFF]-[000]
V	[000]-[FFF]-[0-11]-[-101]-[-101]-[0-11]-[FFF]-[000]
VI	[000]-[FFF]-[1-10]-[0-11]-[0-11]-[1-10]-[FFF]-[000]

3. Simulation and Experimental Results

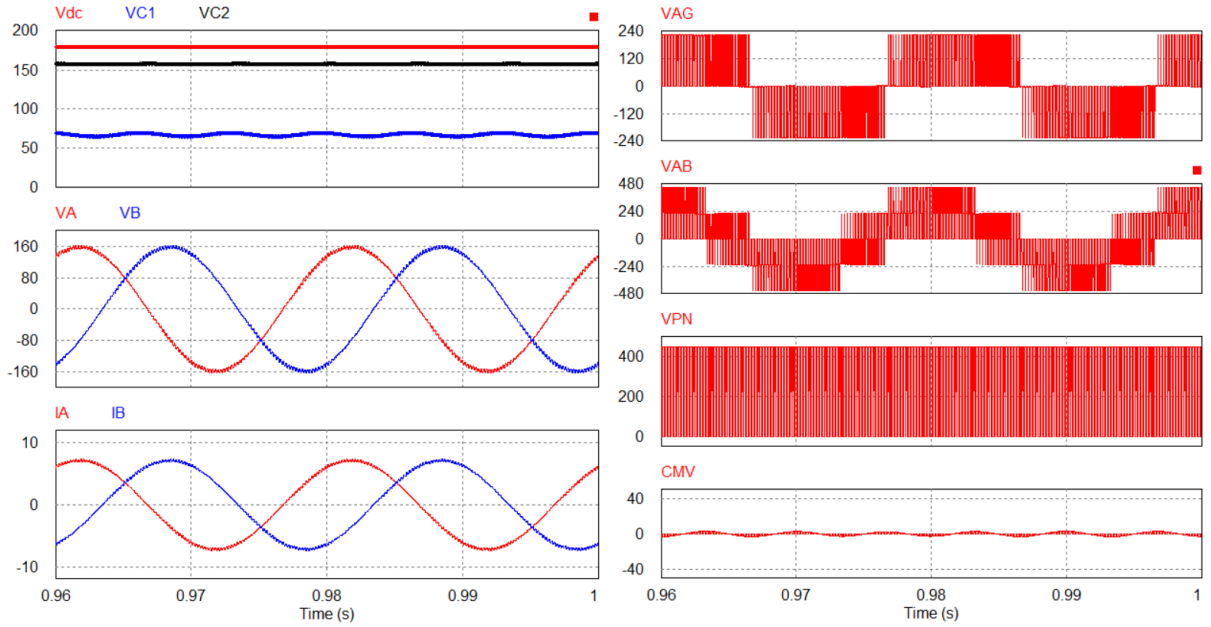
3.1. Simulation Results

Table 5. *Simulation and experiment parameters*

Parameter /	Components	Population
Input voltage	V_{dc}	180 V
Output voltage	$V_{o,RMS}$	110 V_{RMS}
Output frequency	f_0	50 Hz
Carrier frequency	f_s	5kHz
ST duty cycle	D_{ST}	0.3
Modulation index	m	0.7
Boost inductor	L_1, L_2=L_3	3mH, 1mH
Capacitors	C_2=C_3, C_1=C_4	2200µF
LC filter	L-C	3mH- 10µF
Resistor load	R_t	40Ω

The accuracy of the TL-qZSNPCI-ECMV was validated by simulation results with the help of PSIM software. The parameters used for simulation are listed in Table 3. The magnitude of high-frequency harmonics was reduced by using a three-phase low pass filter before feeding to a three-phase resistor load. Table 5 presents the circuit parameters used in the simulation and experiment.

Figure 5(a) shows the simulation results from top to bottom of the input voltage waveform V_{dc} and the voltage waveform on two capacitors, C_1 and C_2. The input voltage value is 180V, the output voltage RMS value, and the output current RMS value. The average voltage of the capacitors C_1 and C_2 measured is 72.5V and 150V, respectively. The measured output voltage and current RMS value is $110V_{RMS}$ and $5A_{RMS}$, respectively.



(a) (b)

Figure 5. *Simulation results for the TL- qZSNPCI-ECMV when Vdc = 180 V and D_{ST} = 0.3.*

The simulation results of the voltage waveform from phase to load neutral point for V_{AG}, V_{AB}, V_{DC_link} voltage waveform, and CMV waveform are shown in Figure 5(b). The simulation results show that the voltage waveform from the phase load V_{AG} has three voltage levels measured with approximate values of +250V, 0V, and -250V. The output line to line voltage has five level of magnitude. The peak of the line to line voltage and the DC-link voltage is 450V. Simulation results show that the RMS value of CMV is $1.56V_{RMS}$.

3.2. Experimental Results

A 1 kW prototype of the TL-qZSNPCI-ECMV was tested in a lab using the same as the simulation, which are shown in Table 5. A DSP F28335 microprocessor and an FPGA Cyclone II EP2C5T144C8 controlled this prototype. The gate-drive was based on TLP250, which fed to IGBT FGL40N150D, which are the low-side and high-side switches of the 3L-T^2I branch. IGBT FGL40N120D and MOSFET 6R045A were installed, respectively, for bidirectional switches and the switches of the qZS network.

Figure 6(a) shows the experimental results from top to bottom of the input voltage waveform. V_{dc}, the voltage waveform on two capacitors, C_1 and C_2, the output voltage RMS value, and the output current RMS value. The input voltage value is 180V, the average voltage of the capacitors C_1 and C_2 measured is 67V and 143V, respectively. The measured output voltage and current RMS value is $106V_{RMS}$ and $5.1A_{RMS}$, respectively.

The experimental results of the voltage waveform from phase to load neutral point for V_{AG}, V_{AB}, V_{DC_link} voltage waveform, and CMV waveform are shown in Figure 6(b). The experimental results show that the voltage waveform from the phase A relative to the load neutral point V_{AG} has three voltage levels measured with approximate values of +240V, 0V, and -240V. The output line to line voltage has

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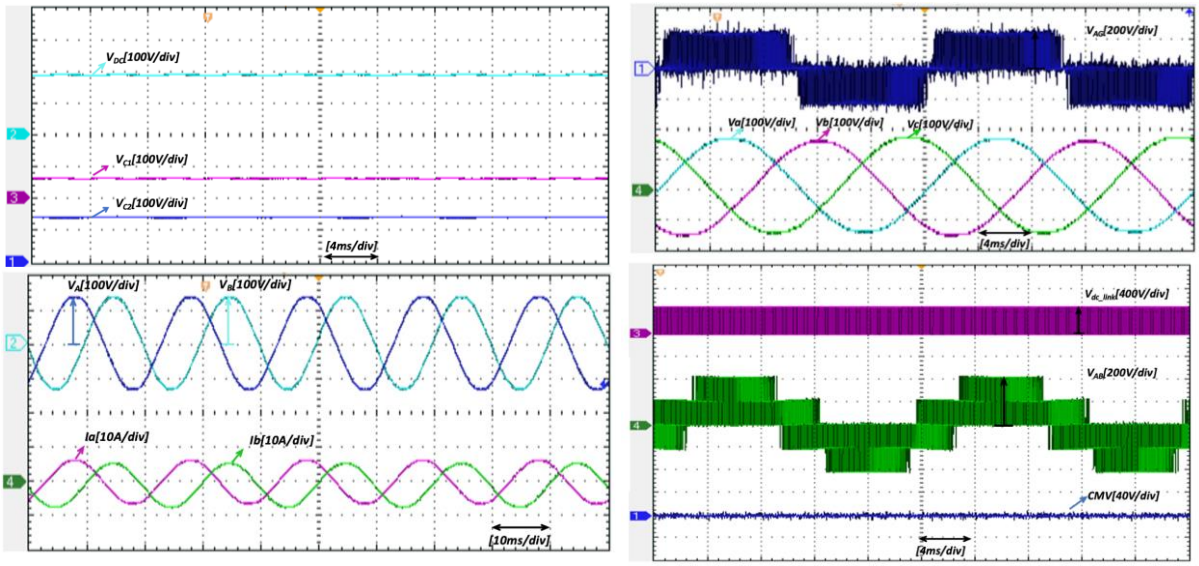
five levels of magnitude. The peak of the line voltage and the DC-link voltage is 440V. The effective value of CMV is $3.2V_{RMS}$.

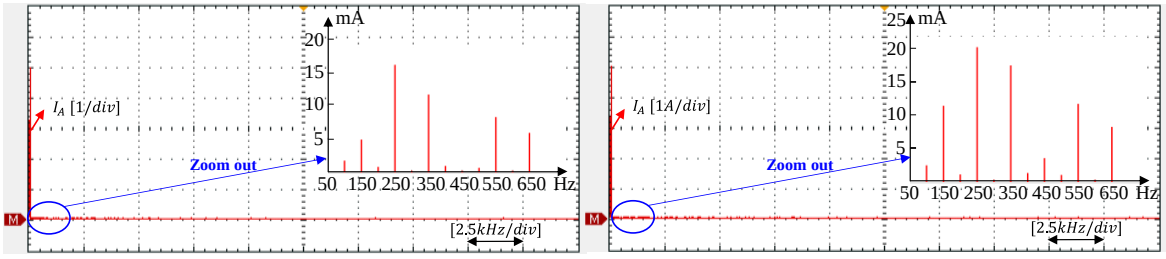
Figure 5 and Figure 6, it can be seen that the experimental results have slightly lower parameters than the simulation results because of the power loss on the circuit board and on the power elements, so the difference between simulation and experimental results is inevitable.



(a) (b)

Figure 6. *Experimental results for the TL- qZSNPCI-ECMV when V_{dc} = 180 V and D_{ST} = 0.3.*

It can be seen that, using the CMV proposed algorithm, the THD of the output phase voltage increases in Figures 6(b). However, the effective value of CMV when using the proposed algorithm decreases significantly, which can be observed in Figures 7 and table 6.



(a) (b)

Figure 7. *The waveform of the FFT spectrum signal of the output current, (a) the output phase voltage spectrum signal of the paper [8]; (b) the output phase voltage spectrum signal of the proposed paper.*

The output load current (I_A) FFT analysis for the two approaches is carried out as shown in Figures 7. When taking into consideration the I_{AG}'s harmonic spectrum, the first order harmonic of the output load current is the same for both methods and is 5.1 A in magnitude. The results of harmonic spectrum calculations are used to derive the THD values of I_A, as given in Table 6. The THD value of the load current is significantly lower than the output phase voltage due to the presence of a three-phase low pass filter at the output. 2.34% and 3.3%, respectively. This THD percentage is still 3.3% below 5% when compared to the IEC61000-4-30 Edition 2 Class A standard, nevertheless.

Table 6. *THD analyses of output load current (THDI).*

	Method in [8]	**Proposed Method**
THD_I	2.34%	3.3%

4. Conclusions

This paper has proposed the SVM technique for the TL-qZSNPCI-ECMV. In the paper, the formulas related to calculating the value of common-mode voltage are also shown in this paper. Based on these formulas, the paper proposed to use medium vectors and zero vector to suppress common-mode voltage. The operating principle of the Space vector algorithm and the traditional PS pulse width modulation technique have been described in detail in the paper and simulated on PSIM software. The common-mode voltage results of the PS algorithms are synthesized and compared with the common-mode voltage of the proposed algorithm. After analysis, the results show that the proposed algorithm is superior to the traditional PS algorithm. The experimental model was operated to verify the presented theories and simulations. The results show that, with no significant deviation, the results of common-mode voltage as well as the values of phase voltage, line to line voltage and output current obtained from the experiment are completely consistent with the results. Simulation and experimental results as well as theory analyzed in the paper. In the near future, this research result will be improved and connected grid.

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