JTE HCMUTE
ISSN: 2615-9740

JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Education
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

F-Type Single Phase Five Level Inverter

Duc-Tri Do*, Vinh-Thanh Tran, Thi Ngoc-Hieu Phu, Van-Hoan Phan
Ho Chi Minh City University of Technology and Education, Vietnam

* Corresponding author. *Email: tridd@hcmute.edu.vn*

ARTICLE INFO

Received: 03/03/2023
Revised: 08/04/2023
Accepted: 17/04/2023
Published: 28/08/2023

KEYWORDS

Multilevel inverter;
DC-AC converter;
F-type inverter;
NPC inverter;
T-type inverter.

ABSTRACT

In modern industrial and power electronics applications, high-voltage and high-current integrated modular power transistors (IGBTs) are increasingly being utilized. The F-type inverter, which is a modified version of the T-type inverter, has emerged as a promising option. This configuration separates the common point of the bidirectional power switch, reducing voltage stress and resulting in lower inverter costs and losses. The F-type inverter has a simplified design and lower conduction losses, making it a viable choice for medium-voltage applications compared to the clamp diode NPC inverter configuration. Detailed analysis of losses and efficiency has been conducted, and a simulation and experimental prototype have been built to validate the theoretical basis. In addition, the voltage rating of the power switches in the T-type three-level inverter is a limiting factor, as it is only 50% of the input DC voltage for each inverter phase leg.

Doi: https://doi.org/10.54644/jte.78A.2023.1357

1. Introduction

The growing demand for electricity in industry and commerce has elevated the importance of renewable energy sources that can be integrated into the grid through inverters. While the traditional two-level voltage source inverter was frequently used in grid-connected applications, the multilevel inverter has increased popularity due to its benefits, including reduced voltage harmonic distortion, lower output current [1]-[3], and the ability to operate at switching frequencies and voltages that are within the range of low power switches [4].

There are three common inverter configurations used today, including H-bridge cascaded inverter (CHB) [5], flying capacitor (FC) [3], and clamped neutral point (NPC) [6]. These three profiles have different features and applications depending on their intended use. H-bridge inverters require symmetric and isolated input sources for each H-bridge, making them suitable for use in multi-source systems [7]. However, generating multilevel voltage using a single input power source is challenging for H-bridge inverters, making them unsuitable for such systems. The traditional NPC inverter and the FC inverter are similar in some ways. Both use the input voltage provided by the capacitor voltage, but the number of output levels and phases in the FC configuration depends on the number of capacitors. This makes the use of many capacitors and high capacitance in the FC configuration a drawback. Therefore, the capacitance cost of the NPC inverter is lower than that of the FC inverter. In addition, the voltage control across the capacitor in the FC configuration is more complex than in the NPC inverter [8].

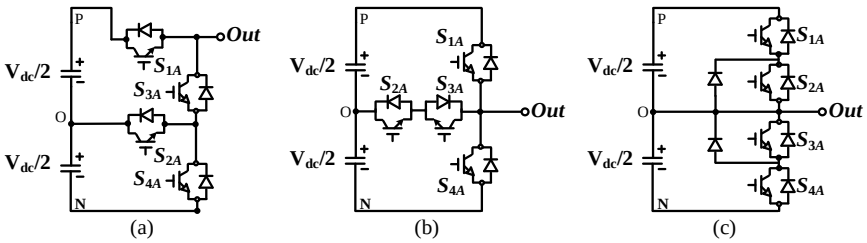


Figure 1. *Single phase inverter, a) F-type inverter, (b) T-type inverter, (c) clamp diode inverter.*

Figure 1 shows three inverter configurations: (a) F-type inverter, (b) T-type inverter, and (c) clamp diode inverter. The clamp diode inverter is a type of inverter that uses clamp diodes to limit the voltage on each phase of the output waveform. This is the foundation of the neutral point clamp (NPC) inverter, which is a type of inverter commonly used in high-power applications. However, the number of clamping diodes required in a clamp diode NPC inverter depends on the number of output voltage levels [9]. On the other hand, the T-type inverter is another type of inverter that has similar features to the NPC inverter. Specifically, the T-type inverter can also provide high-quality output voltage with low harmonic distortion while also offering high efficiency and reliable operation. The T-type inverter has an advantage over the NPC inverter in that it eliminates the need for clamping diodes, which simplifies the design and reduces the number of power components required [9]. The neutral point in the T-type inverter is connected through a bidirectional power switch, and capacitors in series are used on the one-way side. The F-type inverter is a recent variation of the T-type inverter [10], where 25% of the voltage is applied to the power switch, resulting in lower cost and loss compared to the T-type inverter. Like the clamp-diode NPC configuration and T-type inverter, the output voltage of the F-type inverter is determined by the input dc-side capacitor voltage, which must be well balanced to achieve the desired voltage level.

In this paper, the advantages of F-type single-phase 5-level inverters are compared to those of NPC and T-type inverters. It includes operational principles, control techniques, and loss analysis for the three configurations. The research findings are verified using PSIM simulation software and a practical prototype.

2. F-type single-phase inverter

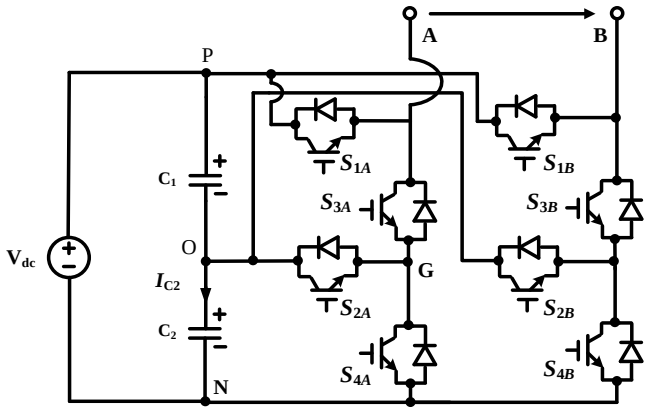


Figure 2. *F-type single phase five level inverter*

The F-type five-level single-phase inverter is a type of inverter that uses a DC input source and two series-connected capacitors (C_1 and C_2) to create a source neutral point (O). By generating a voltage waveform with five levels of magnitude on the output side, it can produce high-quality power. The F-type structure is a modification of the T-type structure, in which the common node of the two power switches connected in series is separated, reducing the number of power switches subjected to the applied voltage V_{dc}.

The F-type five-level single-phase inverter circuit has two-phase branches with four IGBT power switches each: branch A (S_{1A}, S_{2A}, S_{3A}, S_{4A}) and branch B (S_{1B}, S_{2B}, S_{3B}, S_{4B}). S_{1A} and S_{1B} are directly connected between the input and output sides, while the other switches are connected in series. This results in S_{1A} and S_{1B} are faced to the source voltage, while the other switches experiencing to a voltage level equal to 50% of the source voltage during operation.

The advantages of F-type inverters compared to traditional configurations (T-type, NPC) are:

The proposed inverter has a reduced number of power switches compared to the NPC configuration. This feature simplifies the circuit and lowers its costs.

Additionally, compared to the T configuration, the F-type inverter carries fewer power switches to the full DC-link voltage, which may increase the reliability and lifetime of the inverte.

JTE HCMUTE
ISSN: 2615-9740
JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Education
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

As shown in the diagram in Figure 2, because the structure of the two-phase branch is the same, in this part of the operating principle only the states at branch A are considered, and the same for branch B. The F-type five-level inverter operates based on the switching states of the power switches in the two-phase legs A and B. The phase voltage A can reach voltage level "+$V_{dc/2}$" (state "P") when switches S_{1A} and S_{2A} are triggered or voltage level "-$V_{dc/2}$" (state "N") when switches S_{3A} and S_{4A} are triggered. The zero state ("O") is reached when switches S_{2A} and S_{3A} are activated. The output voltage V_{AB} is then formed by combining the voltage levels of both phase legs, producing five voltage levels: +V_{dc}, +$V_{dc/2}$, 0, -V_{dc}, -$V_{dc/2}$.

2.1. Operation principles

Table 1. *Switching states of the inverter*

Mode	S_{1A}, $\overline{S_{3A}}$	S_{2A}, $\overline{S_{4A}}$	S_{1B}, $\overline{S_{3B}}$	S_{2B}, $\overline{S_{4B}}$	V_{AB}
1	1	1	1	1	0
2	1	1	0	1	$+V_{dc}/2$
3	0	1	0	0	$+V_{dc}/2$
4	1	1	0	0	V_{dc}
5	0	1	0	1	0
6	0	1	1	1	$-V_{dc}/2$
7	0	0	0	1	$-V_{dc}/2$
8	0	0	1	1	$-V_{dc}$
9	0	0	0	0	0

In Modes 2-(g), 2-(h), and 2-(i), power switch S_{1A} is connected to the V_{dc} input source along with switches S_{3A} and S_{4A}, resulting in a voltage of V_{dc} across S_{1A}. Similarly, in Modes 3.2-(c), 3.2-(d), and 3.2-(i), power switch S_{1B} is connected to a voltage of V_{dc}. Power switches S_{2x}, S_{3x}, and S_{4x} are connected in series, which results in only half of V_{dc} being applied to them, reducing the system cost, circuit structure, and switching losses of the F-type inverter compared to other types of inverters. To achieve a voltage of +V_{dc}, four switches, S_{1A}, S_{2A}, S_{3B}, and S_{4B}, should be in the "ON" state, while the four switches S_{1B}, S_{2B}, S_{3A}, and S_{4A}, should be in the "OFF" state. To achieve a voltage V_{AB}= +$V_{dc/2}$, either the four switches S_{1A}, S_{2A}, S_{2B}, and S_{3B} should be in the "ON" state, while the four switches S_{1B}, S_{4B}, S_{3A}, and S_{4A} should be in the "OFF" state, or the four switches S_{2A}, S_{3A}, S_{3B}, and S_{4B} should be in the "ON" state, while the four switches S_{1A}, S_{4A}, S_{1B}, and S_{2B} should be in the "OFF" state.

The state 0 of V_{AB} can be achieved in three ways: by turning on four switches (S_{1A}, S_{2A}, S_{1B}, and S_{2B}) while four switches (S_{3A}, S_{4A}, S_{3B}, and S_{4B}) are turned off, or by turning on four switches (S_{2A}, S_{3A}, S_{2B}, and S_{3B}) while four switches (S_{1A}, S_{4A}, S_{1B}, and S_{4B}) are turned off, or by turning on four switches (S_{3A}, S_{4A}, S_{3B}, and S_{4B}) while four switches (S_{1A}, S_{2A}, S_{1B}, and S_{2B}) are turned off. The state of V_{AB}= -$V_{dc/2}$ can be reached by turning on four switches (S_{2A}, S_{3A}, S_{1B}, and S_{2B}) while four switches (S_{1A}, S_{4A}, S_{3B}, and S_{4B}) are turned off, or by turning on four switches (S_{3A}, S_{4A}, S_{2B}, and S_{3B}) while four switches (S_{1A}, S_{4A}, S_{1B}, and S_{4B}) are turned off. Finally, the state of V_{AB}= -V_{dc} can be reached by turning on four switches (S_{3A}, S_{4A}, S_{1B}, and S_{2B}) while four switches (S_{1A}, S_{2A}, S_{3B}, and S_{4B}) are turned off.

The equivalent circuit diagram in Figure 3 illustrates that in Modes 2-(g), 2-(h), and 2-(i) as well as Modes 3.2-(c), 3.2-(d), and 3.2-(i), the power switches S_{1A} and S_{1B} are connected in series with the input source V_{dc} and other switches including S_{3A}, S_{4A}, S_{2x}, S_{3x}, and S_{4x}. Consequently, the voltage across S_{1A} and S_{1B} is either equal to or greater than V_{dc}, while the voltage across the other switches is only half of V_{dc}. This reduction in voltage decreases the system cost, simplifies the circuit structure, and minimizes switching loss in the F-type inverter, making it a more efficient choice than traditional inverters such as the T-type and NPC inverters.

JTE
HCMUTE
ISSN: 2615-9740

JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Education
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

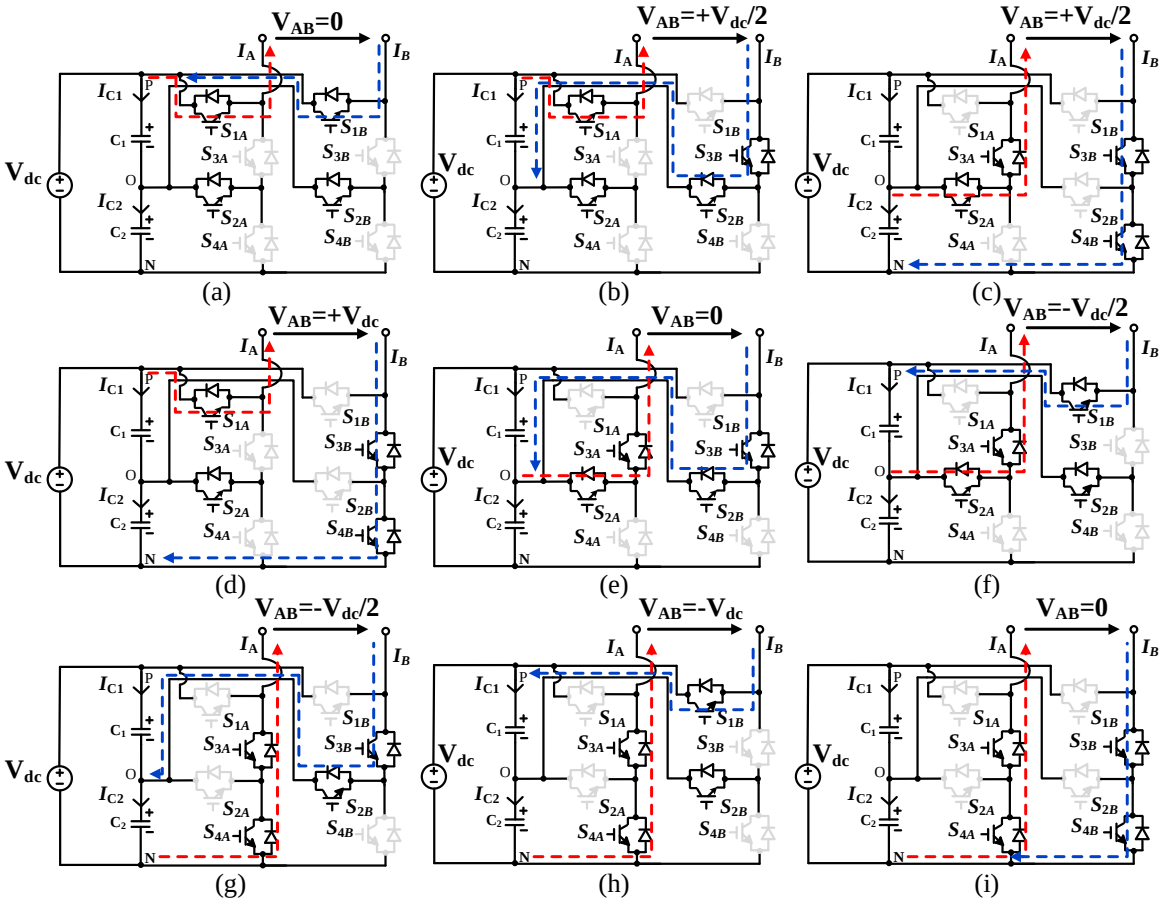


Figure 3. *Equivalent circuit diagram according to Table 1: (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4; (e) Mode 5; (f) Mode 6; (g) Mode 7; (h) Mode 8; (i) Mode 9.*

2.2. Control method

The general equation of the two control waves:

$$\begin{cases} V_a = m.\sin(2\pi ft) \\ V_b = m.\sin(2\pi ft + \pi) = -m.\sin(2\pi ft) \end{cases} \quad (1)$$

Where *f is the desired output frequency (50 Hz); 0 ≤ m ≤ 1 is the modulation index.*

Peak amplitude of the output voltage first harmonic:

$$V_X = m \times V_{dc} \quad (2)$$

Where V_x is the output voltage V_{AB}

The trigger control for power switches is dependent on two control signals (v_a, v_b) and two high-frequency carriers (v_{car1}, v_{car2}), as shown in Figure 4. The control law is presented as:

$$\begin{aligned} S_{1A}, S_{1B} &= \begin{cases} 1 & if \quad v_X > V_{Car1} \\ 0 & else \end{cases} \\ S_{2A}, S_{2B} &= \begin{cases} 1 & if \quad v_X < V_{Car2} \ \ or \ V_{Car2} < v_X < V_{Car1} \\ 0 & else \end{cases} \\ S_{3A}, S_{3B} &= \begin{cases} 1 & if \quad v_X \le V_{Car1} \\ 0 & else \end{cases} \\ S_{4A}, S_{4B} &= \begin{cases} 1 & if \quad v_X < V_{Car2} \\ 0 & else \end{cases} \end{aligned} \quad (3)$$

JTE
HCMUTE
ISSN: 2615-9740

JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Education
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

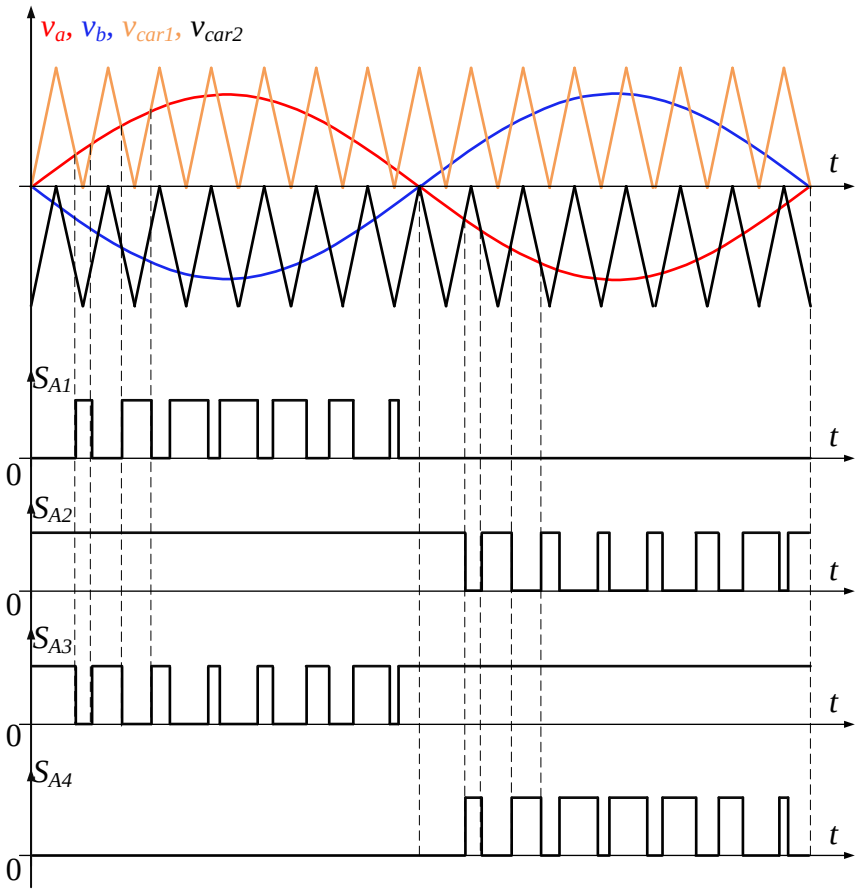


Figure 4. *Control method for phase A.*

2.3. Loss analysis for F-type , T-type, and NPC configurations.

Table 2. *MOSFET technique parameters IPW60R055CFD7*

Parameters	Symbol hiệu	Value	Unit
Nominal Voltage	V_{DS}	650	V
Maximum current	I_D	38	A
Conductor resistor D-S	$R_{DS(on)}$	55	mΩ
Lead time delay	$t_{d(on)}$	26	ns
Rise time	t_r	27	ns
Interrupt delay time	$t_{d(off)}$	98	ns
Reduction time	t_f	5	ns
Forward voltage applied across diode	V_{SD}	1	V
Reverse recovery time	t_{rr}	128	ns
Reverse recovery loss	Q_{rr}	0,77	µC

The switching and conduction losses of the power elements in the inverter circuits are described based on the parameter table of the components and the operating principles of the configurations that are presented are as follows:

Switching loss of power switch S_{1A} and S_{4A}.

$$\begin{cases} P_{onS_{1A}orS_{14A}} = \dfrac{1}{2\pi}.\int_0^{\pi}\dfrac{V_{DC}}{2}.I_{S_{1A}orS_{4A}}(t).\mathrm{t}_{on}.f_s dt \\ P_{offS_{1A}orS_{4A}} = \dfrac{1}{2\pi}.\int_0^{\pi}\dfrac{V_{DC}}{2}.I_{S_{1A}orS_{4A}}(t).\mathrm{t}_{off}.f_s dt \end{cases} \quad (4)$$

Where $t_{on} = t_{(d)on} + t_r$.

Conduction loss of power switch S_{1A} and S_{4A}.

$$P_{cond,S_{1A}\,or\,S_{4A}} = \mathrm{I}^2_{S_{1A}\,\mathrm{or}\,S_{4A},rms}.R_{ds(on),1} \quad (5)$$

Where $R_{ds(on),1}$: value of resistor conduction D-S of switch S_{1A}

Conduction loss of capacitor

$$P_{cond,C} = r_C.\mathrm{I}^2_{C,rms} \quad (6)$$

Where $R_{ds(on),1}$: value of resistor conduction D-S of switch S_{1A}

Where r_C is the value of the parasitic resistance of the capacitor.

Diode conduction loss during reverse recovery (reverse recovery loss).

$$\begin{cases} P_{rr,D_2} = \dfrac{1}{2\pi}.\int_{\pi}^{2\pi}\dfrac{V_{DC}}{2}.f_s.Q_{rr}dt \\ P_{rr,D_3} = \dfrac{1}{2\pi}.\int_0^{\pi}\dfrac{V_{DC}}{2}.f_s.Q_{rr}dt \end{cases} \quad (7)$$

Conduction loss due to dead-time (S_{2A}, S_{3A}).

$$\begin{cases} P_{dead,S_{2A}} = \dfrac{1}{2\pi}.\int_{\pi}^{2\pi}2.V_{SD}.\left|I_{S_{2A}}(t)\right|.t_{dead}.f_s dt \\ P_{dead,S_{3A}} = \dfrac{1}{2\pi}.\int_0^{\pi}2.V_{SD}.\left|I_{S_{3A}}(t)\right|.t_{dead}.f_s dt \end{cases} \quad (8)$$

From Equation (4) to Equation (8) the total losses of F-type inverter, T-type inverter and NPC inverter are presented as follows:

$$\begin{aligned} \sum P_{loss} = {} & P_{onS_{1A}} + P_{onS_{4A}} + P_{offS_{1A}} + P_{offS_{4A}} + P_{rr,D_2} + P_{rr,D_3} + P_{dead,S_{2A}} + P_{dead,S_{3A}} \\ & + P_{cond,C} + P_{cond,S_{1A}} + P_{cond,S_{2A}} + P_{cond,S_{3A}} + P_{cond,S_{4A}} \end{aligned} \quad (9)$$

From equation (4) to equation (9), the statistical combinations of the parameters in Table 2 and switching losses are as shown in Figures 5 and 6.

Figures 5 and 6 present the losses of the inverters, in which the inverter has a total loss including: conduction loss and switching loss. Conduction losses include: conduction losses across clamping diodes; power switch conduction losses; and capacitor conduction losses. Losses on clamping diodes provide for 34.37% of conduction losses in NPC inverter; conduction losses on power switches also made for a significant portion of losses in NPC inverter with a ratio of 29.78%, the remaining conduction loss on the capacitor reach for 20.07%, and the switching loss only reach for about 15.79% of the total loss on the circuit (Figure 5c). For the T-type inverter, the conduction losses of the four power switches reach for the largest share of the circuit losses, up to 51.05%, while the conduction losses on the

capacitors and the switching losses reach for about half of the total losses. The switching losses are 27.16% and 24.57%, respectively (Figure 5b). The loss ratio in F-type inverter is also similar to that in T-type, where the conduction loss on the switches provides for the largest percentage of 50.66%. The loss on the capacitor is 27.57%, and the lowest proportional switching loss in the F-type inverter is 21.09% (Figure 5a).

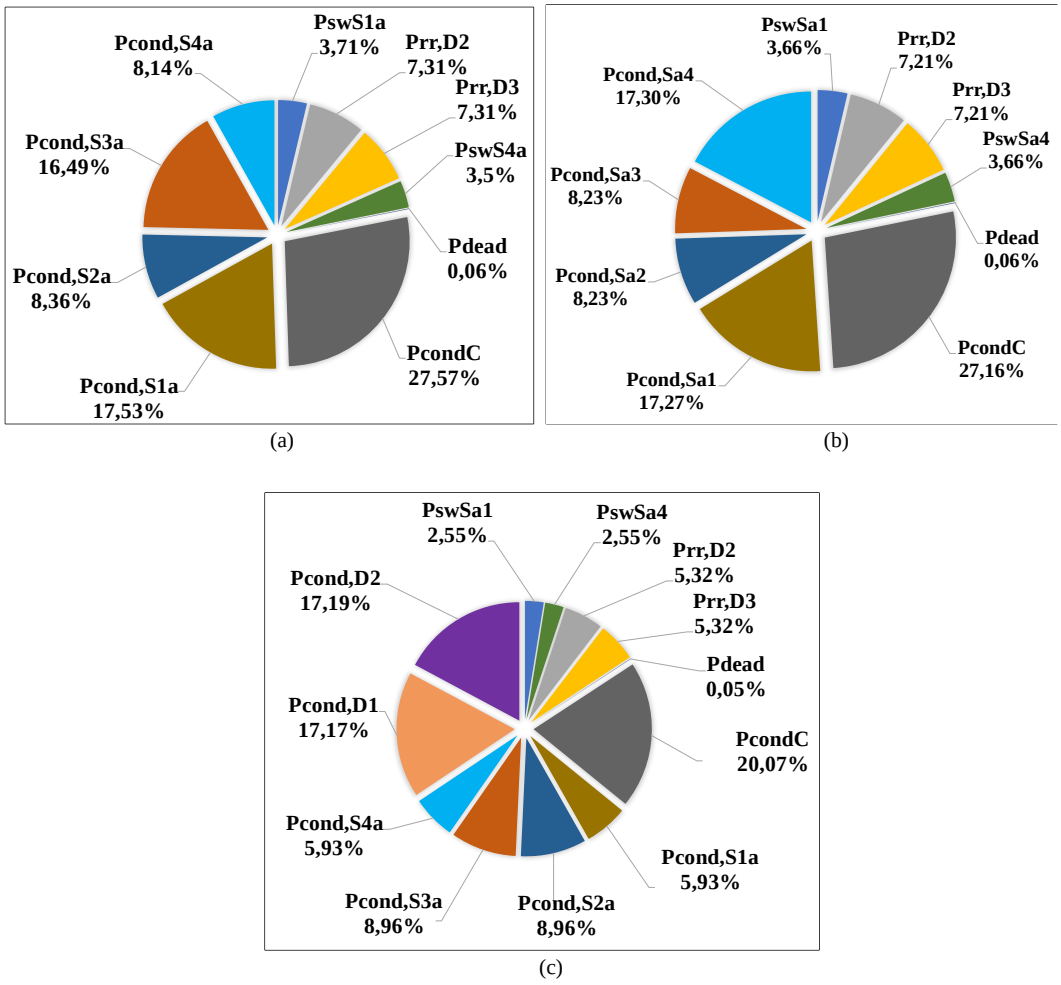


Figure 5. *Information about each loss component in the inverter circuit: (a) Configuration F-type; (b) Configuration T-type; (c) NPC Configuration.*

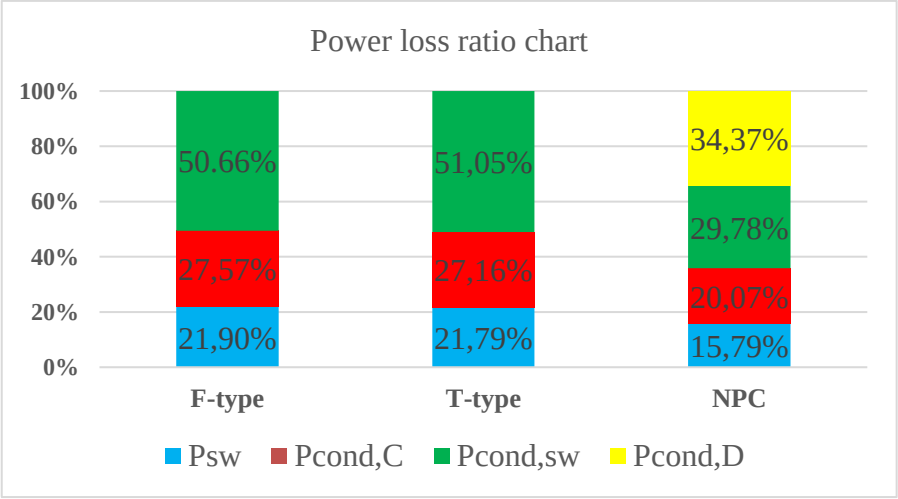


Figure 6. *Ratio of loss components in each configuration.*

Thus, the F-type inverter is more efficient than the NPC and T-type inverters, reducing loss by about 27.2% and 1.5%, respectively, when compared to the NPC inverter. Losses are greatly reduced compared with the NPC inverter because the F-type inverter has eliminated clamping diodes. However, when compared with the T-type inverter, the F-type inverter has a negligible loss, but in terms of the operating principle of the F-type inverter, the voltage applied to the power switch has been reduced by 50% compared with the T-type inverter. Therefore, compared to the other two topologies, T-type and NPC, the F-type five-level single-phase inverter has the maximum efficiency with the parameters in Table 3.

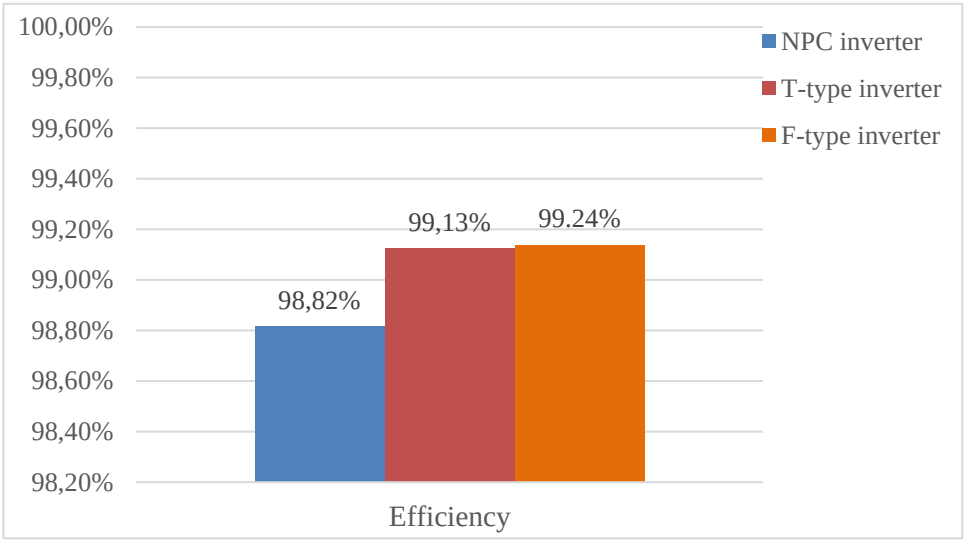


Figure 7. *Efficiency of F-type, T-type, and NPC inverter.*

As shown in Figure 7, the F-type inverter has the best efficiency, reaching 99.24%. The T-type inverter then achieves a computational efficiency of 99.13%, which is nearly equal to that of the F-type inverter. The NPC inverter has the lowest performance in the calculation. This shows that the F-type inverter has improved the loss and efficiency of the circuit compared to the NPC and T-type inverter.

3. Simulation and Experimental Results

To evaluate the performance of the converter. The control parameters of the inverter are shown in Table 3:

Table 3. *Simulation and experiment parameters*

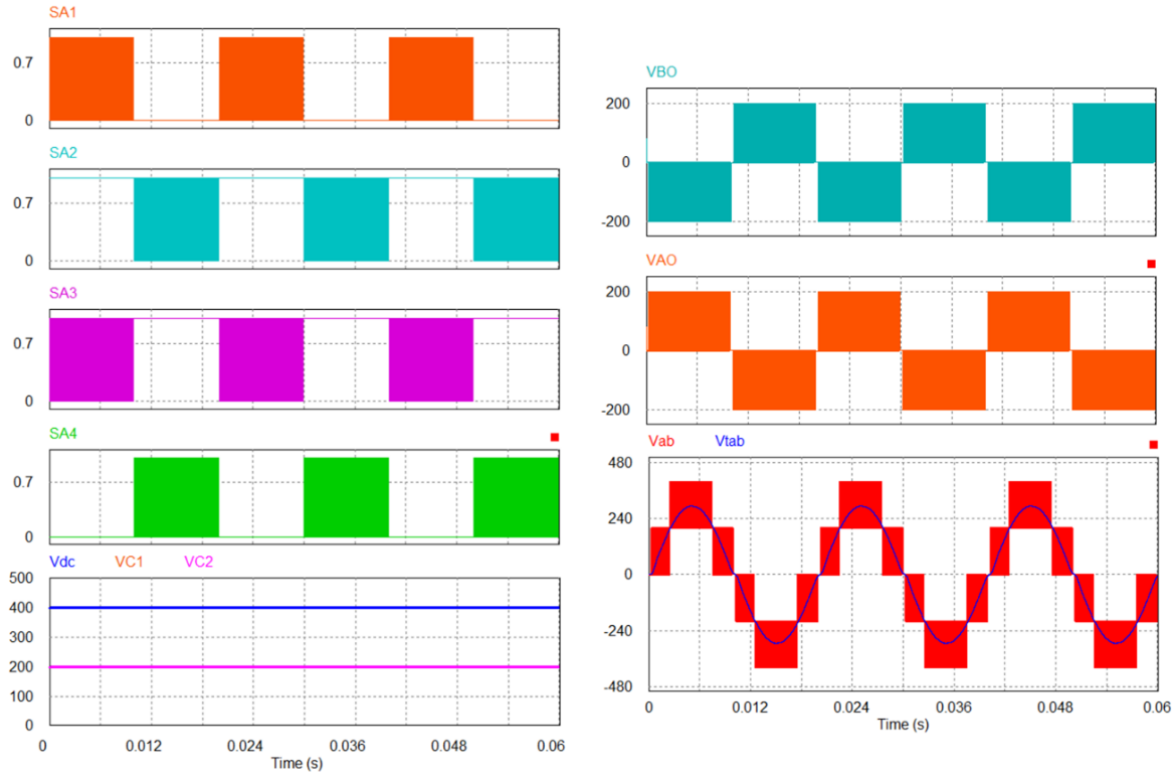
Parameter/Components		Unit
Input voltage	V_{dc}	400 V
Output voltage	$V_{AB,RMS}$	220 V_{RMS}
Output frequency	f_0	50 Hz
Carrier frequency	f_s	10 kHz
Modulation index	m	0.78
LC filter	L-C	3mH- 10µF
Resistor load	R_t	12.1Ω

In Figure 8(a), from top to bottom, we can see the control signal waveforms of power switches for phase A (S_{1A}, S_{2A}, S_{3A}, and S_{4A}), the input voltage (V_{dc}), and the voltage across capacitors C_1 and C_2. It is apparent that the S_{1A} power switch is phase-shifted by 180 degrees compared to the S_{3A} power switch, and similarly, the S_{2A} power switch is phase-shifted by 180 degrees compared to the S_{4A} power switch. The input voltage is 400V, and the voltage across capacitors C_1 and C_2 is 200V each.

JTE
HCMUTE
ISSN: 2615-9740

JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Education
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

In Figure 8(b), from top to bottom, the phase voltages A_0, B_0, and the output line-to-line voltages are shown before and after passing through the LC filter. The output phase voltage of phase A is phase-shifted by 180 degrees compared to phase B, with a peak amplitude of 200V. The peak amplitude of the output line-to-line voltage is 400V, and the RMS line-to-line voltage is 220V.



(a) *(b)*

Figure 8. *Simulation results of a single-phase 5-level F-type inverter: (a) control signal waveforms of phase A (S_{1A}, S_{2A}, S_{3A}, S_{4A}), voltage across capacitors C_1 and C_2, (b) phase voltage waveforms (V_{A0}, V_{B0}) and line voltage (V_{AB}) before and after filtering.*

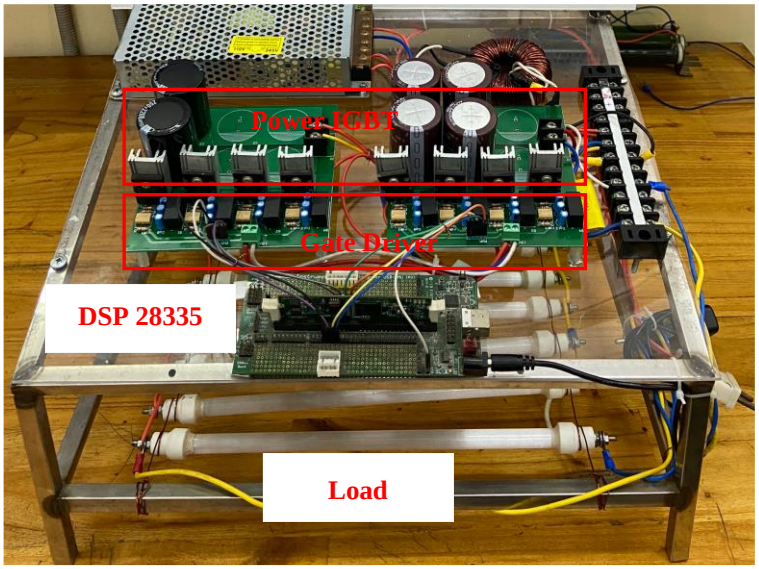
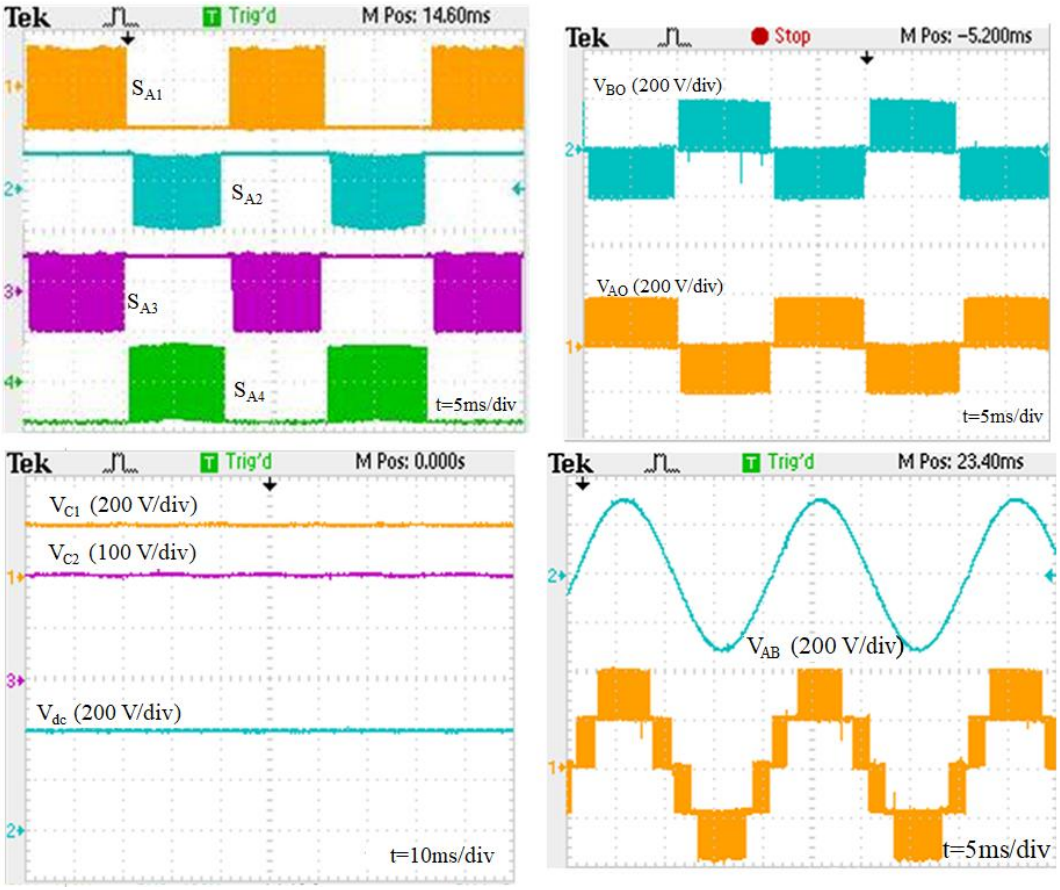


Figure 9. *Prototype of a F-type five-level single-phase inverter.*

JTE
HCMUTE
ISSN: 2615-9740

JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Education
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

The efficacy of the PWM strategy under investigation has been verified through experiments carried out on a laboratory prototype, as shown in Figure 9. The experimental parameters were identical to those used in the simulations, thus ensuring accurate verification. IGBTs FGL40N150 were employed for the inverter leg, specifically for S_{1A} to S_{4A} and S_{1B} to S_{4B}.



(a) *(b)*

Figure 10. *Experimental results of a single-phase 5-level F-type inverter: (a) control signal waveforms of phase A (S_{1A}, S_{2A}, S_{3A}, S_{4A}), voltage across capacitors C_1 and C_2, (b) phase voltage waveforms (V_{A0}, V_{B0}) and line voltage (V_{AB}) before and after filtering.*

Similar to the simulation results shown in Figure 8, Figure 10 (a) has an input voltage of 400V, and the voltages across capacitors C_1 and C_2 are 193V and 191V, respectively. In Figure 10(b), the peak amplitude of the output phase voltage is 192 V. The peak amplitude of the output line voltage is 384V, and the RMS line-to-line voltage is 216V. The unfiltered output line voltage, V_{AB}, has a magnitude of five levels, while the line voltage through the filter is a sine wave. However, the experimental result has a lower voltage value than the simulation result due to the voltage drop across the power elements in the prototype.

4. Conclusions

This paper presents the advantages of the F-type single-phase 5-level inverter in comparison to the NPC and T-type inverters. The operational principles, control techniques, and loss analysis for the five-level inverter are discussed. The results of the loss study indicate that the F-type inverter reduces loss by 27.2% compared to the NPC inverter and 1.5% compared to the T-type inverter. The research findings were demonstrated using PSIM software and a prototype. However, this study was limited to a 4 kW load capacity, and the application of the F-type inverter at higher load power would result in significantly improved efficiency and reduced losses.

Acknowledgments

This work was supported by the Advanced Power Electronics Laboratory D405, with the support of the T2023-63 project at Ho Chi Minh City University of Technology and Education, Viet Nam.

List of Acronyms

5L	Five level
PWM	Pulse Width Modulation
NPC	Neutral Point Clamped
CHB	Cascaded H-Bridge
FC	Flying Capacitor
IGBT	Integrated Modular Power Transistors
T^2I	T-Type Inverter

REFERENCES

[1] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
[2] D. T. Do, V. T. Tran, and M. K. Nguyen, "Enhanced Boost Factor for Three-Level Quasi-Switched Boost T-Type Inverter," *Energies*, vol. 14, no. 13, pp. 1-17, 2021.
[3] S. Laamiri, M. Ghanes, and G. Santomenna, "All-silicon 99.35% efficient three-phase seven-level hybrid neutral point clamped/flying capacitor inverter," *Trans. Pow. Electron. App.*, vol. 4, no. 1, pp. 50–61, 2019.
[4] J. Bhatnagar and V. Dave, "A comparative study of different topologies of multilevel inverters," *Int. J. Electron. Electron. Eng.*, vol. 9, no. 01, pp. 2050-2056, 2017.
[5] D. T. Do, V. T. Tran, and N. A. Truong, "Single-phase five-level quasi-switch boost inverter with high voltage gain," *Measurement, Control, and Automation*, vol. 1, no. 1, pp. 1-8, 2020.
[6] D. T. Do, "A Single-Stage Neutral Point Clamp Inverter with Reduced Voltage Stresses on Power Elements," *Measurement, Control, and Automation*, vol. 2, no. 2, pp. 24-31, 2021.
[7] R. Kumar and D. Thangavelusamy, "A modified nearest level modulation scheme for a symmetric cascaded H-bridge inverter," *Gazi Univ. J. Sci.*, vol. 32, no. 2, pp. 471-481, 2019.
[8] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197-2206, Jul. 2010.
[9] D. T. Do, V. T. Tran, M. K. Nguyen, and S. Naik, "Fault Tolerant Control Methods for Three-Level Boost T-Type Inverter," *IEEE Trans. Ind. Electron.*, Early Access, Aug. 2022.
[10] A. A. Elserougi, I. Abdelsalam, and A. Massoud, "Five-level F-type inverter with buck-boost converter-based equalization channels," *Alexandria Engineering Journal*, pp. 1-17, 2022.

Do Duc Tri was born in Vietnam in 1973. He received the B.S., M.S. and Ph.D degrees in electronic engineering from the Ho Chi Minh City University of Technology and Education, Ho Chi Minh City, Vietnam, in 1999, 2012 and 2021, respectively. He is currently a Lecturer with the Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology and Education. His current research interests include power converters for renewable energy systems.

Tran Vinh Thanh was born in Viet Nam, in 1995. He received the B.S. and the M.S degrees in Electronic Engineering from Ho Chi Minh City University of Technology and Education, Viet Nam, in 2018 and 2020, respectively. He currently working toward the Ph.D. degree in Electronic Engineering at Ho Chi Minh City University of Technology and Education, Viet Nam. His current research interests include impedance source inverter and control of multi-level inverter.

Phu Thi Ngoc Hieu was born in Viet Nam, in 1981. She received B.S degree in Control Engineering and Automation from the Ho Chi Minh City University of Technology, Viet Nam, in 2004 and M.S degree in Control Engineering and Automation, in 2008, from the Ho Chi Minh University City of Technology. She has currently been being a Lecturer of the Faculty of Electrical and Electronic Engineering at Ho Chi Minh City University of Technology and Education since 2011. Her current research interests include Automatic Control and Power Electronic.

Phan Van Hoan was born in Vietnam in 1986. He graduated from Ho Chi Minh City University of Technology and Education with a B.S degree in Electrical and Electronics Engineering in 2009 and a M.S degree in Electronic Engineering in 2011. Since 2012, he has been a lecturer in the Faculty of Electrical and Electronics at Ho Chi Minh City University of Technology and Education. His current research interests include Industrial Electronics and Power Electronics.