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A New 3-Phase 2-Level Buck Inverter with Switching Loss Improvement

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ABSTRACT

This paper proposes a 3-phase 2-level inverter configuration combined with a buck DC-DC converter to improve the switching loss of semiconductor devices. Compared to the traditional 3-phase 2-level inverter configuration, this configuration can reduce the number of switching times on the inverter side by about 2/3 compared to the sine Pulse Width Modulation technique (sine PWM) and 1/2 compared to the Discontinuous PWM (DPWM). Different from traditional configurations and techniques (DC-link voltage is constant), this configuration controls DC-link voltage to change and equal to the maximum pole voltage on the inverter side. Hence, the phase with the maximum and minimum voltages has no switching. In addition, compared to traditional techniques, the switching voltage of the switches inverter side is also significantly decreased. To verify the advantage of reducing switching loss, the simulation results of power loss analysis were performed using PSIM and PLECS software and experimented on the experimental model. In experimental results, when the output power is 900 W, the proposed configuration efficiency is 3.36% larger than the traditional configuration.

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1. Introduction

Three-phase DC/AC inverter systems for electronic equipment are currently in high demand, finding applications in various fields including motor speed control [1], [2], fast charging systems [3], [4], and PV solar battery systems [5]. Among these systems, 3-phase 2-level voltage source inverters are widely utilized due to their advantages such as a simple configuration, low cost, and compact size.

The 3-phase 2-level voltage source inverter usually uses the Sine Pulse Width Modulation (sine-PWM) technique [6]. In this technique, the switches are controlled to turn on and off based on the sine-shaped control signal for all three phases. The advantage of the sine-PWM technique is simple and easy to use. However, it also has a drawback: the modulation index (M) is limited to $M \leq 1$. Additionally, each phase branch of the inverter produces switching losses on the switches within each carrier period. Therefore, when the circuit operates at a high switching frequency, the semiconductor loss in the circuit is very large, leading to a reduction in the conversion efficiency of inverter. To address these switching losses, a discontinuous PWM (DPWM) technique has been proposed [7], [8]. In this technique, the control voltage of the semiconductor switch is obtained by subtracting the minimum phase voltage from each phase voltage. As a result, the phase with the lowest instantaneous voltage remains connected to the negative point of the DC-link voltage. Therefore, there is no switching loss on the switches of this phase branch. The DPWM technique reduces switching losses by 33% when compared to the sine-PWM technique. In addition to reducing the switching loss, the DPWM technique also allows for an increase in the modulation index (M) of up to approximately 1.15.

Although the DPWM technique offers several advantages, such as an improved modulation index and reduced switching losses for the traditional two-level inverter configuration, it also has some drawbacks, which are presented as follows. Firstly, both the sine-PWM and DPWM techniques maintain a DC-link voltage equal to the input DC voltage of the inverter. However, the DC-link voltage is typically much higher than the output AC voltage. Consequently, despite the implementation of DPWM, the switching losses of semiconductor devices remain relatively high due to the high DC-link voltage. Secondly, on the phase branch operating with the highest instantaneous output voltage, switching losses

still occur within each carrier period. This is also one of the causes leading to the increase in switching losses.

In recent years, with the development of semiconductor technologies, such as silicon carbide (SiC) and Gallium Nitride (GaN), has led to the development of semiconductor switches that offer high-frequency operation and reduced switching losses compared to traditional silicon-based devices [9]. Inverter circuits constructed with SiC or GaN semiconductor devices exhibit improved efficiency and power density. However, the cost associated with these components is considerably higher than that of traditional ones. As a result, hybrid inverters have been proposed to combine the benefits of low-loss SiC/GaN devices with the cost-effectiveness of Si devices [9]-[11]. Nevertheless, these hybrid inverters use quite a lot of Si and SiC components, resulting in limited improvements in factors such as circuit cost and size.

This paper introduces a new inverter circuit that combines the buck DC-DC converter with the traditional 3-phase 2-level inverter to address switching losses on the inverter side. The DC-DC circuit utilizes SiC components, while the DC-AC circuit is built using Si-IGBTs. In this inverter circuit, the DC-link voltage on the inverter side is controlled to be equal to the output AC voltage, thereby reducing the switching voltage of the inverter semiconductor switches (Si-IGBT). In addition, the phase operating with the maximum and minimum instantaneous voltages experiences no switching on the switches. As a result, the total number of reverse switching instances can be reduced by approximately 2/3 compared to the sine-PWM technique [6] and about 1/2 compared to the DPWM technique [7], [8]. The following sections of the paper will provide detailed information on the proposed inverter configuration, control technique, power loss analysis, and comparative results. The structure of the paper consists of four parts: Part II - the proposed circuit configuration, Part III - parameters for component selection, Part IV - simulation, experimental, and comparative results, and Section V - the conclusion of the paper.

2. The proposed circuit configuration

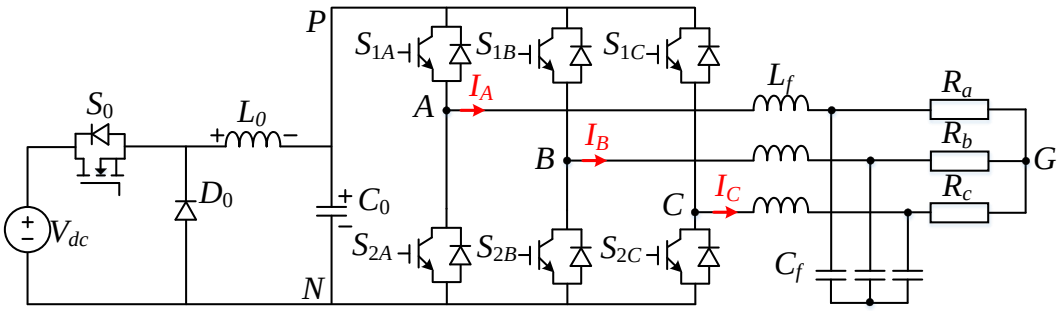

Figure 1. *Configuration of a 3-phase 2-level buck inverter*

As shown in Fig. 1, the proposed configuration includes a buck DC-DC converter and a 3-phase 2-level inverter. The buck DC-DC converter consists of a positive semiconductor switches S_0, inductor L_0, capacitor C_0, and diode D_0. The 3-phase 2-level inverter consists of three branches, each branch has two switches, S_{1X} and S_{2X}. The output pole voltage of V_{XN} (X is A, B, C) has two voltage levels: V_{PN} and 0-V. When the switch S_{1X} is closed, the output pole voltage is $+V_{PN}$. The output pole voltage reaches 0-V when the switch S_{2X} is closed. The operation of the proposed inverter circuit is analyzed based on the operation of the DC-DC circuit and the DC-AC circuit as follows.

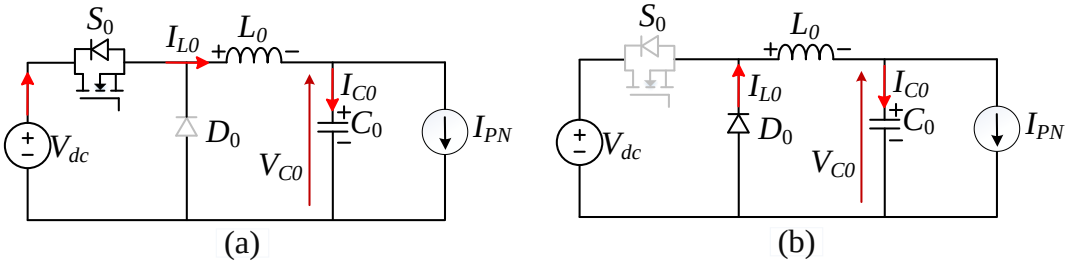

Figure 2. *Operating principle of the buck DC-DC converter. (a) state 1, (b) state 2*

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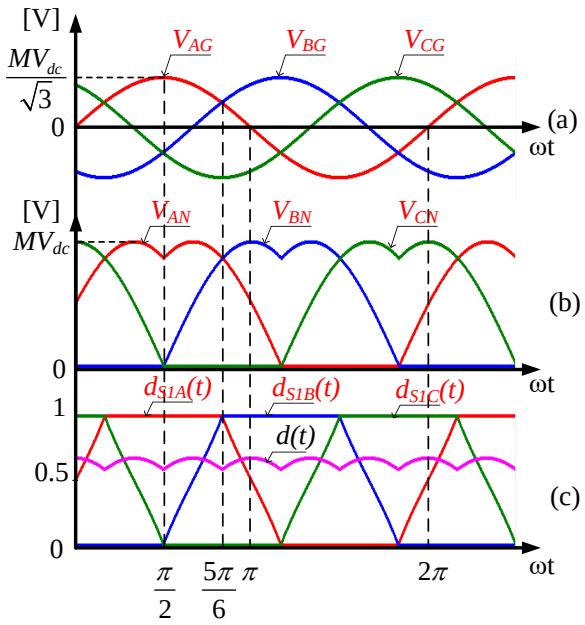

Figure 3. *Proposed DPWM technique*

2.1. Operation principle of DC-DC stage

The buck DC-DC converter circuit has two operating states, as shown in Figures 2(a) and 2(b). In state 1, the switch S_0 is closed, diode D_0 has reverse bias, and the DC power supplies energy to the inductor L_0. The voltage across the inductor L_0 and the current through the capacitor C_0 are presented as:

$$\begin{cases} V_{L0} = L_0 \dfrac{di_{L0}}{dt} = V_{dc} - V_{C0} \\ I_{C0} = C_0 \dfrac{dv_{C0}}{dt} = I_{L0} - I_{PN} \end{cases} \quad (1)$$

In which: V_{dc}, V_{L0}, and V_{C0} are the input voltage, the voltage of inductor L_0 and the voltage of capacitor C_0, respectively.

In state 2, the switch S_0 is interrupt enabled. Diode D_0 is forward biased, and capacitor C_0 load energy from the input DC power supply to inductor L_0. The voltage across the inductor L_0 and the current through the capacitor C_0 are represented as:

$$\begin{cases} V_{L0} = L_0 \dfrac{di_L}{dt} = -V_{C0} \\ I_{C0} = C_0 \dfrac{dv_C}{dt} = I_{L0} - I_{PN} \end{cases} \quad (2)$$

Assume that in each switching period $T_S = 1/f_S$, the switch S0 is activated with a duty cycle $d(t)$. It can be seen that the action times of mode 1 and mode 2 are $d(t)T_S$ and $[1\text{-}d(t)]T_S$, respectively. Similar to the traditional buck DC-DC circuit [12], the voltage across the capacitor C_0 can be represented as follows:

$$V_{C0}(t) = V_{dc}.d(t) \quad (3)$$

2.2. Operation principle of DC-AC stage

The first harmonic of the output phase voltage $V_{XG,1}$ is defined as follows:

$$\begin{cases} V_{AG,1}(t) = M \times V_{dc} \sin(\omega t)/\sqrt{3} \\ V_{BG,1}(t) = M \times V_{dc} \sin(\omega t - 2\pi/3)/\sqrt{3} \\ V_{CG,1}(t) = M \times V_{dc} \sin(\omega t + 2\pi/3)/\sqrt{3} \end{cases} \quad (4)$$

Where $\omega = 2\pi f$ is the angular frequency and f is the frequency of the output voltage.

To generate the output phase voltage as shown in (4), the pole voltage $V_{XN,1}$ shown in Figure 3(b), is defined as follows:

$$\begin{cases} V_{AN,1}(t) = V_{AG,1} + V_{off} \\ V_{BN,1}(t) = V_{BG,1} + V_{off} \\ V_{CN,1}(t) = V_{CG,1} + V_{off} \end{cases} \quad (5)$$

The voltage V_{off} is defined as:

$$V_{off} = -\min(V_{AG,1}, V_{BG,1}, V_{CG,1}) \quad (6)$$

In order to reduce the switching loss of the semiconductor switches on the inverter side, the DC-link voltage is controlled to equal the maximum value of $V_{XN,1}$, as shown in Figure 3(b). Based on (3) and (5), the duty cycle of the switch S_0 is calculated as follows:

$$d(t) = \frac{\max(V_{AN,1}, V_{BN,1}, V_{CN,1})}{V_{dc}} \quad (7)$$

At this time, the DC-link voltage is cyclic with a period $T/6$, where T is the load voltage period. During $[\pi/2 - 5\pi/6]$, the voltage on capacitor C_0 is equal to the pole voltage at phase A. Therefore, the switch S_{1A} is controlled by duty cycle 1. The remaining semiconductor switches for phases B and C (S_{1B} and S_{1C}) are controlled at the ratio of $V_{XN,1}$ to V_{C0}. In short, the duty cycles of S_{1A}, S_{1B}, and S_{1C} switches are calculated as follows:

$$\begin{cases} d_{S1A}(t) = \dfrac{V_{AN,1}}{\max(V_{AN,1}, V_{BN,1}, V_{CN,1})} \\ d_{S1B}(t) = \dfrac{V_{BN,1}}{\max(V_{AN,1}, V_{BN,1}, V_{CN,1})} \\ d_{S1C}(t) = \dfrac{V_{CN,1}}{\max(V_{AN,1}, V_{BN,1}, V_{CN,1})} \end{cases} \quad (8)$$

It can be seen that for each 1/6 of the load voltage period, the phase with the maximum and minimum pole voltage has no switching on the semiconductor switches. The other phase operates with a switching frequency equal to the switching frequency of the inverter side. It can be concluded that the number of reverse switching times is reduced by about 2/3 compared to the traditional sine-PWM technique [6] and by 1/2 compared with the DPWM scheme proposed in [7] , [8].

3. Component Selections

3.1. Inductor and Capacitor Selections

The output load current I_X in one period T is defined as follows:

$$\begin{cases} I_A(t) = I_m \sin(\omega t) \\ I_B(t) = I_m \sin(\omega t - 2\pi/3) \\ I_C(t) = I_m \sin(\omega t + 2\pi/3) \end{cases} \quad (9)$$

where I_m is the peak value of the output load current.

Based on (2), (3) and (7), the current ripple ΔI_{L0} of inductor L_0 is calculated as follows:

$$\Delta I_{L0}(t) = \left| \frac{V_{dc} d(t)[1-d(t)]}{L_0} \times T_S \right| \tag{10}$$

In the time range of [π/2 - 5π/6], duty cycle is calculated as follows:

$$d(t) = \frac{V_{AG,1}(t) - V_{CG,1}(t)}{V_{dc}} = -M \times \cos(\omega t + \pi/3) \tag{11}$$

From (9) and (10), the current ripple value ΔI_{L0} of the inductor L_0 reaches its maximum value at ωt = 2π/3. Therefore, the maximum value of the current ripple through the inductor $\Delta I_{L0,\max}$ is calculated as:

$$\Delta I_{L0,\max}(t) = \left| \frac{V_{dc} \times M(1-M)}{L_0} \times T_S \right| \tag{12}$$

During [π/2 - 5π/6], based on (1), (2) and (8), the average current through the inductor I_{L0} in any switching period T_S is calculated as follows:

$$\bar{I}_{L0,Ts}(t) = \bar{I}_{PN,Ts}(t) = I_A(t)[1-d_{S1B}(t)] - I_C(t) d_{S1B}(t) \tag{13}$$

In the range of [π/2 - 5π/6], we have the maximum value of $V_{AN,1}$ and the minimum value of $V_{CN,1}$. based on (5), (6) and (8) determine as:

$$d_{S1B}(t) = \frac{V_{BG,1} - V_{CG,1}}{V_{AG,1} - V_{CG,1}} = \frac{\cos(\omega t)}{\cos(\omega t + \pi/3)} \tag{14}$$

Based on (9), (13) and (14), the average value of current through the inductor L_0 calculated in any switching period reaches the maximum value at $\omega t = \pi/2$, calculated as follows:

$$\bar{I}_{L0,Ts,\max} = I_m \tag{15}$$

The inductor L_0 is selected in term of $\Delta I_{L0,max} \le k_L\%\ \bar{I}_{L0,Ts,\max}$, where k_L% is maximum acceptable inductor current ripple.

$$L_0 \ge \left| \frac{V_{dc}(1-M) \times M \times T_s}{k_L\% I_m} \right| \tag{16}$$

Based on (1) and (2), the voltage ripple of capacitor C_0 in one switching period is expressed as:

$$\Delta V_{C0}(t) = \frac{V_{dc} d(t)[1-d(t)]}{8 L_0 C_0} \times T_s^2 \tag{17}$$

Replace (11) with (17), and the maximum voltage ripple value $\Delta V_{C0,max}$ of the capacitor C_0 can be calculated as follows:

$$\Delta V_{C0,max} = \left| \frac{V_{dc} M(1-M)}{8 L_0 C_0} \times T_s^2 \right| \tag{18}$$

From (3), the maximum value of the voltage across the capacitor $V_{C0,max}$ can be calculated as follows:

$$V_{C0,\max} = M \times V_{dc} \tag{19}$$

The capacitor C_0 is selected in term of $\Delta V_{C0,max} \le k_C\%\ V_{C0,max}$, where k_C% is maximum acceptable capacitor voltage ripple.

$$C_0 \ge \left| \frac{(1-M)}{k_c\% 8 L_0} \times T_s^2 \right| \tag{20}$$

3.2. Semiconductor device stress

The voltage stresses of the switch S_0 and diode D_0 are the input voltage. The maximum current through the switch S_0 and diode D_0 is the maximum current through the inductor L_0 determined at (15).

$$\begin{cases} V_{S0,rating} = V_{D0,rating} = V_{dc} \\ I_{S0,rating} = I_{D0,rating} = \mathrm{I}_{L0,\max} = I_m \end{cases} \quad (21)$$

The voltage stresses of the switches S_{1X} and S_{2X} are equal to the voltage across the capacitor C_0. The maximum current through the switches is equal to the maximum current of the load $I_{load,max}$.

$$\begin{cases} V_{Sjx,rating} = V_{C0,\max} = M \times V_{dc} \\ I_{Sjx,rating} = \mathrm{I}_{load,\max} = I_m \end{cases} \quad (22)$$

where $j = 1 \div 3$ and $X = A, B, C$.

4. Simulation and Experimental Results

4.1. Simulation Results

The proposed circuit is simulated using PSIM and PLECS software. The simulation parameters are presented in Table 1. The input DC voltage is 400-V. To achieve an output voltage of 110-V_{RMS}, the modulation index M on the inverter side is calculated to be 0.68 for both configurations. The simulation results for the proposed configuration are shown in Figures 4 and 5.

Table 1. *Simulation and experiment parameters*

Parameter/Components		**Unit for simulation and experimentation**	
		Proposed configuration	Traditional configuration
Input voltage	V_{dc}	400 V	400 V
Output phase voltage	$V_{0,RMS}$	110 V_{RMS}	110 V_{RMS}
Output frequency	f_0	50 Hz	50 Hz
DC - DC Buck converter			
MOSFET	S_0	IMZ120R060M1H 1200 V – 60 mΩ	Unavailable
Diode	D_0	UJ3D1250K2 1200V – 1.5V	
Inductor	L_0	1.5 mH, r_L = 66 mΩ	
Capacitor	C_0	10 µF, r_{ESR} = 7.64 mΩ	
The switching frequency of S_0	f_{S0}	10 kHz	
3-phase 2-level inverter			
Modulation ratio	M	0.68	0.68
IGBT	S_{XA}, S_{XB}, S_{XC}	FGL40N150D 1500V – 3.5 V	FGL40N150D 1500V – 3.5 V
Switching frequency	f_s	20 kHz	20 kHz
Filter circuit	C_f và L_f	10 µF and 3 mH	10 µF and 3 mH
Resistor	R	40 Ω	40 Ω

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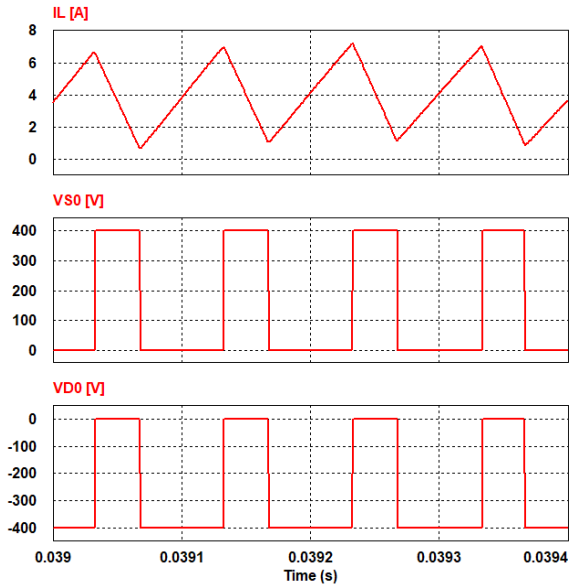

Figure 4. *Simulation results inductor current L_0 (I_{L0}), voltage on switch S_0 (V_{S0}) and voltage on diode D_0 (V_{D0}).*

As shown in figure 4, the current ripple ΔI_{L0} is approximately 6-A and the average measured current is 3.3-A. The voltage across the switches S_0 and diode D_0 is the input voltage of 400-V.

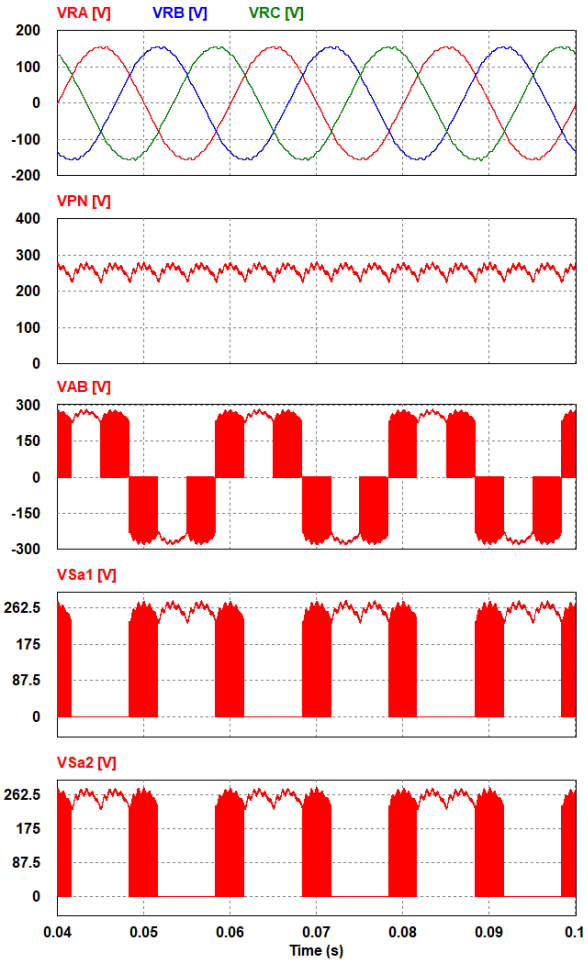

Figure 5. *Simulation results for the proposed configuration. From top to bottom are respectively the phase voltages on the resistive load (V_{RA}, V_{RB}, V_{RC}), the voltage on the capacitor C_0 (V_{PN}), the line-to-line voltage V_{AB}, the voltage across the switches S_{1A}, S_{2A} (V_{S1A},V_{S2A}).*

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The simulation results of the proposed configuration and the traditional configuration are shown in Figures 5 and 6, respectively. As shown in Figure 5, the output load voltages V_{RA}, V_{RB}, V_{RC} are sinusoidal waveforms with the help of the three-phase low-pass filter (3-mH and 10-µF) as listed in Table 1. The RMS values of output load voltages are measured as 110-V_{RMS}. The voltage across the capacitor V_{C0} = V_{PN} has a peak value of 279-V and is cyclic with a period of 1/6 of the load voltage period. The output line-to-line voltage V_{AB} has 3 voltage levels, ± V_{PN}, and 0-V. The voltage stresses on the switches S_{1A}, S_{2A} are equal to V_{PN} = 279-V.

In Figure 6, the RMS values of the output load voltages V_{RA}, V_{RB}, V_{RC} are 110-V_{RMS}. The output line-to-line voltage V_{AB} fluctuates between ±400-V and 0-V. The voltage stresses on the switches S_{1A}, S_{2A} have a value of 400-V.

From Figures 5 and 6, when comparing the proposed configuration and the 3-phase 2-level inverter configuration with the traditional DPWM technique, the output voltage on the load is 110-V_{RMS}, the THD values of the output voltage of the proposed and traditional configurations are 1.7% and 1.76%, respectively. Observing the voltages on the switches S_{1A} and S_{2A} in both configurations, we see that the number of switching times in the proposed configuration is less than that of the traditional configuration, thereby reducing the switching loss on the switches S_{XA}, S_{XB}, S_{XC}. Details are presented below.

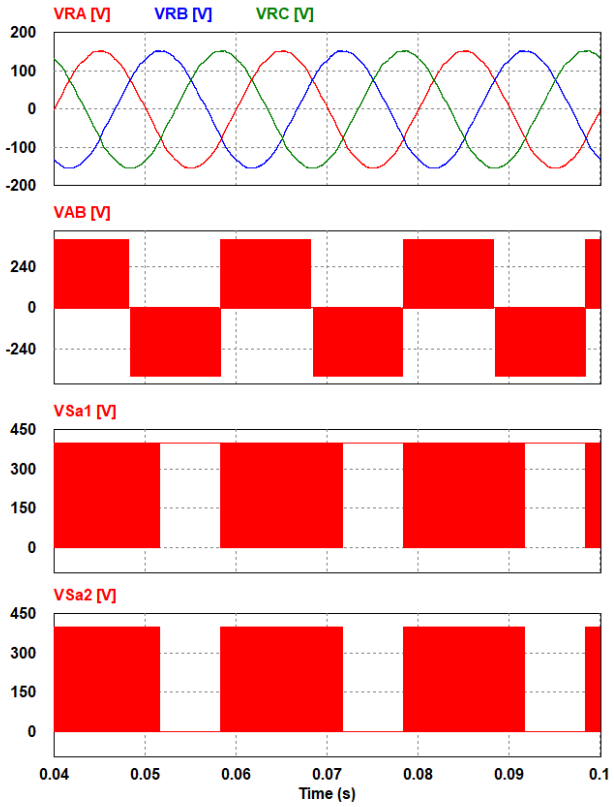
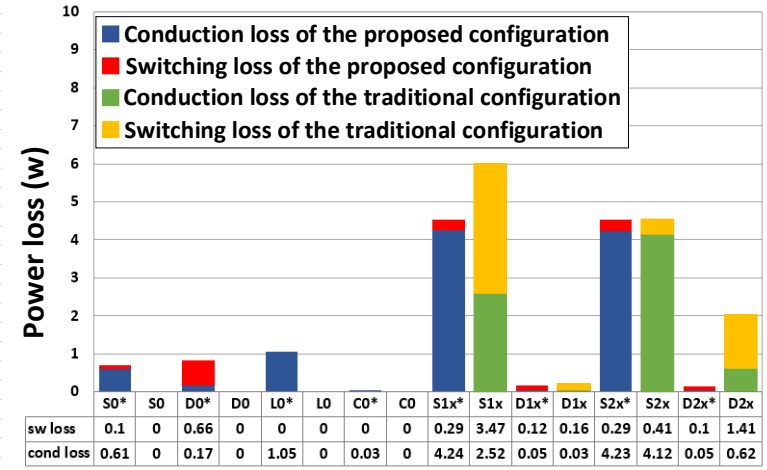


Figure 6. *Simulation results for the traditional configuration. From top to bottom are respectively the phase voltages on the resistive load (V_{RA}, V_{RB}, V_{RC}), the line-to-line voltage V_{AB}, the voltage across the switches S_{1A}, S_{2A} (V_{S1A},V_{S2A}).*

The power losses caused to the circuit include the conduction loss of the inductor (ignoring the core loss of the inductor), the capacitor and the losses of the semiconductor components. The Power loss simulation of the configuration is performed using PLECS software. The simulation parameters are presented in Table 1. Figure 7 shows the simulation results of the power loss components of the proposed configuration and the traditional configuration. The switching loss of the switch S_{1A} in the proposed configuration is reduced by 91.6% compared to the traditional configuration. For the switch S_{2X} , the switching loss of the proposed configuration is 70% of that of the traditional configuration. In addition, the boby diode D_{2X} of the traditional configuration has a reverse recovery loss 14 times larger than in the proposed configuration. The total power loss of the proposed configuration is 30.7-W and the traditional configuration is 38.2-W. Thus, the proposed configuration reduces power loss by 19.63% compared to the traditional configuration.



	S0*	S0	D0*	D0	L0*	L0	C0*	C0	S1x*	S1x	D1x*	D1x	S2x*	S2x	D2x*	D2x
sw loss	0.1	0	0.66	0	0	0	0	0	0.29	3.47	0.12	0.16	0.29	0.41	0.1	1.41
cond loss	0.61	0	0.17	0	1.05	0	0.03	0	4.24	2.52	0.05	0.03	4.23	4.12	0.05	0.62

Figure 7. *The simulation results show power losses for both the proposed and traditional configurations. Among them, (*) only contains the recommended components for configuration. The rest are components of the traditional configuration. (D_{jX} is the diode body of the switch S_{jX}, where j=1 ÷ 3 and X=A, B, C.).*

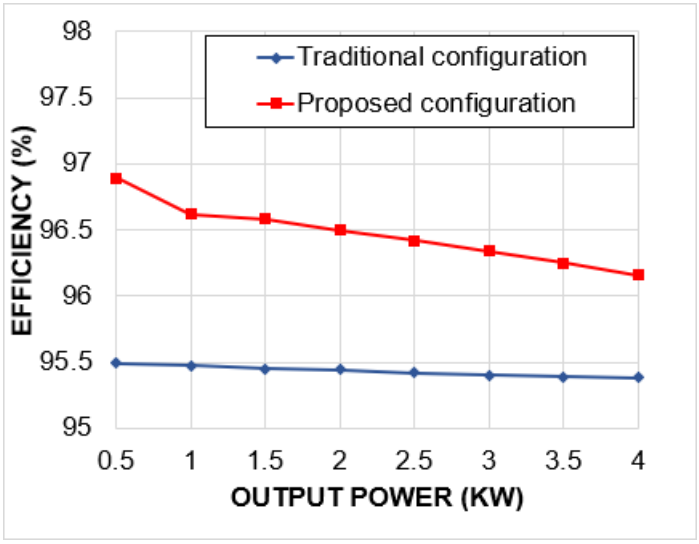


Figure 8. *The efficiency simulation results between the proposed configuration and the traditional configuration.*

With an output voltage of 110-V_{RMS}, the performance simulation results between the proposed configuration and the traditional configuration are shown in Figure 8. It can be seen that the proposed configuration has greater efficiency than the traditional configuration. Since the switching losses on the switches on the inverter side are significantly reduced in the proposed circuit configuration, the efficiency of the proposed configuration is higher than that of the traditional configuration. At the output power of 4-kW, the proposed configuration is 0.78% more efficient than the traditional configuration.

4.2. Experimental Results

It is recommended to use the parameters shown in Table 1 and the experimental model shown in Figure 9 for both the recommended and traditional configurations for experiments. The parameters of the components, semiconductor switches, and diodes are shown in Table 1. The DSP TMS320F28335 microcontroller is used to generate switch control PWM signals for IGBT and MOSFET semiconductor switches. In these two configurations, the input DC voltage is 400-V and the modulation index M is 0.68 to achieve 110-V_{RMS} output AC voltage. The experimental results of these two configurations are shown in Figures 10 and 11.

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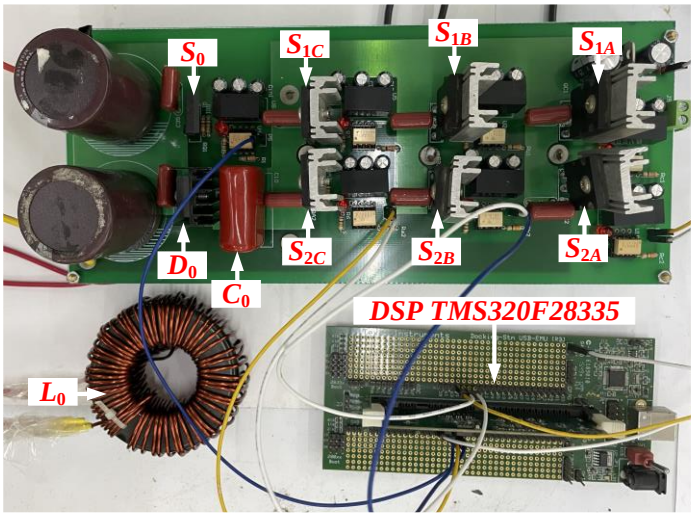

Figure 9. *Experimental model.*

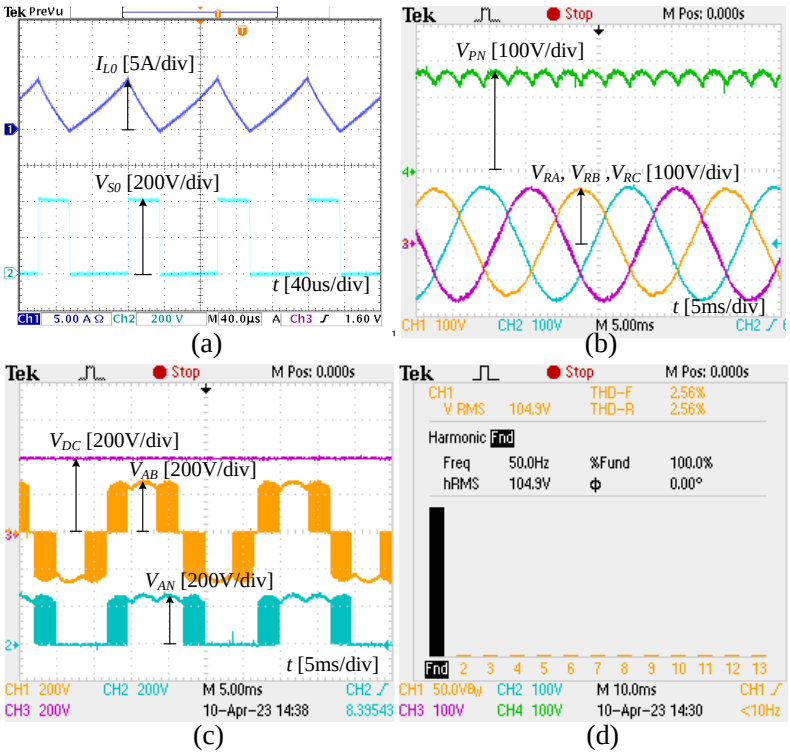

Figure 10. *Experimental results for the proposed configuration. (a) The current through inductor L_0 (I_{L0}) and the voltage across switch S0 (V_{S0}). (b) The voltage on capacitor C_0 (V_{PN}) and the voltage on loads V_{RA}, V_{RB}, V_{RC}. (c) the input voltage V_{DC}, the line voltage V_{AB} and the pole voltage V_{AN}. (d) THD of the V_{RA} voltage.*

The experimental results of the proposed configuration are described as shown in Figure 10. In the buck DC-DC converter, when the switch S_0 is closed, the current through the inductor L_0 increases. When the switch S_0 is tripped, the current through the inductor decreases, as shown in Figure 10(a). The voltage stresses on the switch S_0 are equal to the input DC voltage, whose value is 400-V. The current through the inductor L_0 has an average measured value of 3.36-A. Figure 10(b) shows the output voltage on the loads V_{RA}, V_{RB}, V_{RC} with RMS values of 105-V_{RMS}, 110-V_{RMS}, and 109-V_{RMS} respectively. The RMS value of the voltage across the capacitor C_0 (V_{PN}) measured is 256-V_{RMS}, the THD of the output voltage on the V_{RA} load is 2.56% as shown in Figure 10(d). The output line-to-line voltage V_{AB} has 3 voltage levels: ±V_{PN} and 0-V. The V_{AN} pole voltage has 2 voltage levels: +V_{PN}, 0-V, as shown in Figure 10(c).

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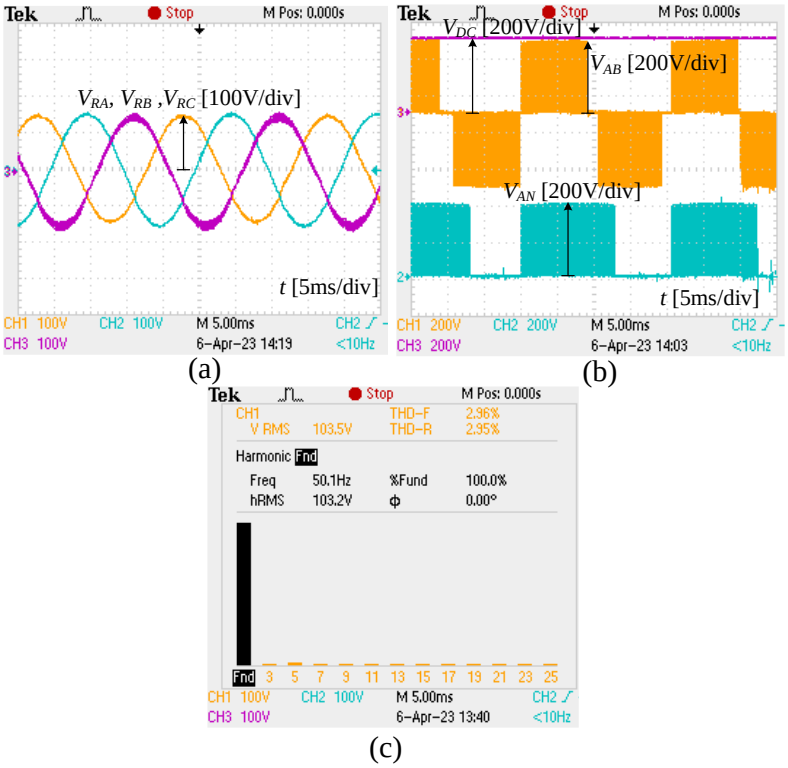

Figure 11. *Experimental results for the traditional configuration. (a) The voltage on capacitor C_0 (V_{PN}) and the voltage on loads V_{RA}, V_{RB}, V_{RC}. (b) the input voltage V_{DC}, the line voltage V_{AB} and the pole voltage V_{AN}. (c) THD of the V_{RA} voltage.*

Figure 11 presents the experimental results of the traditional configuration with the DPWM technique. In figure 11(a) output voltage on load V_{RA}, V_{RB}, V_{RC} has RMS values of 104-V_{RMS}, 109-V_{RMS}, 107-V_{RMS} respectively, and THD of the output voltage V_{RA} is 2.96%, as shown in figure 11 (c). In Figure 11(b), the output line-to-line voltage V_{AB} has three voltage levels: ± 400-V and 0-V. The pole voltage V_{AN} has two voltage levels: + 400-V and 0-V.

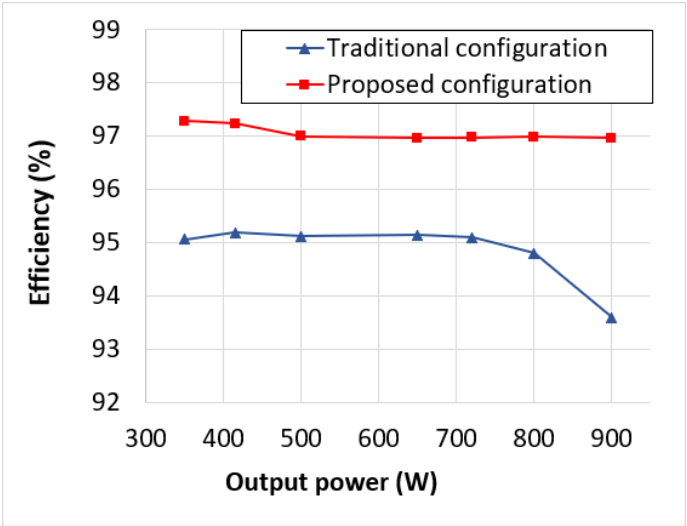

Figure 12. *The efficiency experimental results between the proposed configuration and the traditional configuration.*

The experimental results of the performance between the proposed configuration and the traditional configuration are shown in Figure 12. The performance of the model is measured by a power analyzer WT3000E. It can be seen that the performance of the inverter circuit is improved in the proposed

configuration compared to the traditional configuration. When the output power is 900-W, the proposed configuration efficiency is 3.36% greater than the traditional configuration.

5. Conclusions

This paper presents a technique for the proposed configuration, which is a combination of the buck DC - DC converter circuit and 3-phase 2-level inverter circuit, in order to reduce switching loss and improve circuit efficiency. The theory and operating principle of the proposed configuration have been presented and verified through the simulation results performed by PSIM and PLECS software and experiments with the experimental model. Simulation and experimental results show that the number of switching times on the semiconductor switches on the inverter side of the proposed configuration is reduced compared to the traditional configuration, and the efficiency of the proposed configuration is also larger than that of the traditional configuration. It shows that the switching loss on the semiconductor switches has been improved and that the power loss has been significantly reduced. Configuration suitable for small and medium power applications such as: PV systems, fuel cells, and engines.

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Table 2. *List of Acronyms*

2L	Two level
DPWM	Discontinuous Pulse Width Modulation
SiC	Silicon Carbide
GaN	Gallium Nitride
SinePWM	Sine Pulse Width Modulation
IGBT	Integrated Modular Power Transistors
PV	Photovoltaic

Conflict of Interest

The authors declare no conflict of interest.

REFERENCES

[1] T. M. Jahns and H. Dai, "The past, present, and future of power electronics integration technology in motor drives," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 3, pp. 197 - 216, Sep. 2017.

[2] A. Stippich *et al.*, "Key components of modular propulsion systems for next generation electric vehicles," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 4, pp. 249-258, Dec. 2017.

[3] R. Khezri, P. Razmi, A. Mahmoudi, A. Bidram, and M. H.cKhooban, "Machine Learning-Based Sizing of a Renewable-Battery System for Grid-Connected Homes With Fast-Charging Electric Vehicle," *IEEE Transactions on Sustainable Energy.*, vol. 14, no. 2, pp. 837 - 848, Apr. 2023.

[4] P. Franzese *et al.*, "Fast DC Charging Infrastructures for Electric Vehicles: Overview of Technologies, Standards, and Challenges," *IEEE Transactions on Transportation Electrification*, (Early Access). 2023.

[5] S. Bouguerra, M. R. Yaiche, O. Gassab, A. Sangwongwanich, and F. Blaabjerg, "The impact of PV panel positioning and degradation on the PV inverter lifetime and reliability," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 3114–3126, Jun. 2021.

[6] J. W. Kolar, H. Ertl, and F. C. Zach, "3-Ph 2- Level VSI with Sinusoidal Pulse Width Modulation," in *International Conference for Convergence in Technology*, Pune, India, 2018, pp. 1-4, doi: 10.1109/I2CT.2018.8529565.

[7] W. Li *et al.*, "Implementation of Five-Level DPWM on Parallel Three-Level Inverters to Reduce Common-Mode Voltage and AC Current Ripples," *IEEE Transactions on Ind App.*, vol. 56, no. 4, pp. 4017 - 4027, Aug. 2020.

[8] D. T. Do, V. T. Tran, and M. K. Nguyen, "An DPWM for Active DC-Link Type Quasi-Z-Source Inverter to Reduce Component Voltage Rating," *Energies*, vol. 15, no. 13, p. 4989, Jul. 2022.

[9] C. Liu *et al.*, "Hybrid SiC-Si DC–AC Topology: SHEPWM Si-IGBT Master Unit Handling High Power Integrated With Partial-Power SiC-MOSFET Slave Unit Improving Performance," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 3085-3098, Mar. 2022.

[10] Q. X. Guan *et al.*, "An Extremely High Efficient Three-Level Active Neutral-Point-Clamped Converter Comprising SiC and Si Hybrid Power Stages," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8341-8352, Oct. 2018.

[11] Y. Wang, M. Chen, C. Yan and D. Xu, "Efficiency Improvement of Grid Inverters With Hybrid Devices," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7558-7572, Aug. 2019.

[12] R. S. Ortigoza, V. M. H. Guzmán, M. A.Cruz, and D. M. Carrillo, "DC/DC Buck Power Converter as a Smooth Starter for a DC Motor Based on a Hierarchical Control," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 1076-1084, Feb. 2015.

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