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A Single-Phase Common-Ground Buck – Boost Inverter

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ABSTRACT

This paper presents a new single-phase inverter topology capable of eliminating common-mode voltage (CMV) called the Single-Phase Common Ground Boost/Buck-Boost Inverter (1P-CG-BBI), which aims to overcome the limitations of traditional common ground systems. The PWM algorithm is specifically designed to switch the devices for both DC-DC and DC-AC operations without interfering with each other, with the goal of enhancing voltage regulation and improving energy conversion efficiency. In this topology, a proportional integral (PI) controller is designed to adjust the DC voltage from the Boost/Buck-Boost circuit and the AC voltage from the inverter circuit. By analyzing small signals and optimizing the controller parameters, the system achieves high stability and quick response to load changes. Compared to traditional control topologies, the application of PI in the 1P-CG-BBI topology not only enhances control capabilities but also minimizes energy losses, thereby improving the overall efficiency of the system. The simulation and experimental results in this paper demonstrate the stability and ability to adjust voltage values in both DC-DC and DC-AC operations enabled by the PI controller.

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1. Introduction

The use of renewable energy sources has become a significant trend in pursuing sustainability and mitigating environmental impacts. Inverters are essential components in solar renewable energy systems, as they convert DC voltage from PV panels/fuel cells into AC voltage to supply loads [1]. Among these, the H-bridge inverter topology is one of the most widely used transformerless inverter topologies due to its low production cost, simple control process, and optimized conversion efficiency [2], [3]. However, this topology generates a common-mode voltage (CMV) with a high rate of voltage change (dv/dt), which leads to leakage currents through the parasitic capacitance between the PV/fuel cells and the load's neutral. This effect causes electromagnetic interference (EMI) [4], [5], reduces insulation lifespan, distorts the output current, and affects system stability and quality.

As are presented in Figure 1(a)-1(b), studies [6] and [7], the H5-D inverter was developed by incorporating a grounded diode into the conventional H5 topology. This modification significantly reduces the leakage current amplitude by maintaining the CMV at a constant value. While this topology reduces leakage current, the conversion efficiency is also lowered due to the additional switches. In [8], the HERIC inverter topology was proposed to minimize leakage current while maintaining high conversion efficiency. However, while this topology decreases leakage current, it does not completely eliminate it.

The common-ground (CG) inverter topology eliminates leakage current by maintaining a zero common-mode voltage. However, it operates only as a buck DC-AC inverter, making it unsuitable for PV systems with wide DC input voltage ranges. In contrast, the semi-ZSI inverter structure [9] (semi-impedance source inverter), combined with a DC-DC boost converter, enables both voltage boosting and bucking. This integration creates a flexible CG inverter topology capable of adjusting output voltage amplitude.

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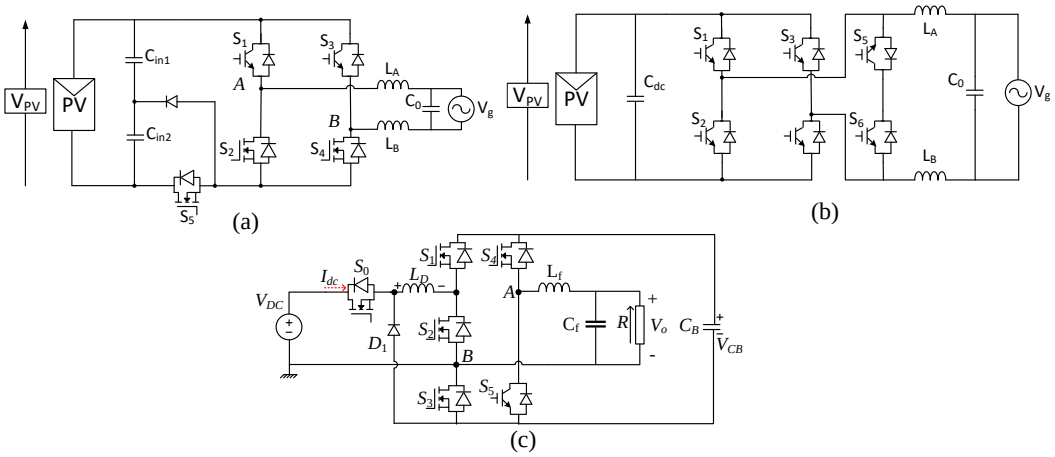

Figure 1. *Inverter topologies. (a) Topology of H5-D [6], [7] (b) Topology of HERIC [8] (c) 1P-CG-BBI proposed topology.*

With the single-phase common ground buck-boost inverter (CG-BBI-1P) topology proposed by our group, it combines the advantages of transformerless inverters, saving space and reducing system costs. Additionally, incorporating a buck-boost DC-DC converter preceding the inverter enables operation over a wide and flexible voltage range. The common ground feature eliminates CMV and minimizes electromagnetic interference (EMI). This configuration is an evolution and development of previous designs, leveraging their advantages while addressing their disadvantages. The paper is structured into four sections: the introduction is presented in section 1, the proposed 1P-CG-BBI topology is detailed in section 2, simulation and experimental validation are covered in section 3, and the conclusion is provided in section 4.

2. 1P-CG-BBI proposed topology

2.1. Steady-state analysis

As depicted in Fig. 1(c), the proposed 1P-CG-BBI configuration consists of a conventional buck-boost DC-DC converter (comprising switches S_0, S_1, S_2, S_3, diode D_1, inductor L_B, and capacitor C_B) and two additional switches, S_4, S_5, which function as a single-phase DC-AC inverter. A low-pass filter (L_f and C_f) is installed before the resistive load to reduce the amplitude of high-frequency harmonic components in the output voltage (V_{AB}). It can be observed that the output load and the DC input source share a common ground, ensuring that there is no leakage current in the proposed configuration.

The proposed configuration operates in 8 distinct modes, as illustrated in Figures 2(a)–2(h). The inverter is controlled separately during the positive and negative half-cycles. The control signals for the switches are depicted in Figure 3.

The operation of the proposed inverter is divided into DC-DC and DC-AC operations. These two phases are independently controlled and detailed as follows. First, the operation of the DC-DC stage is analyzed. During the positive half-cycle, modes 1-4 are applied.

As shown in Figures 2(a)-2(d), switches S_0 and S_3 are always gated on, diode D_1 is not conducting in these four modes. The capacitor C_B is discharged by the current I_{PN}. The voltage across the inductor L_B and the current through the capacitor C_B are calculated as follows:

$$\begin{cases} V_{LB} = L_B \dfrac{di_{LB}}{dt} = V_{dc} \\ I_{CB} = C_B \dfrac{dv_{CB}}{dt} = -I_{PN} \end{cases} \quad (1)$$

Where I_{PN} is the equivalent current of the DC-AC side.

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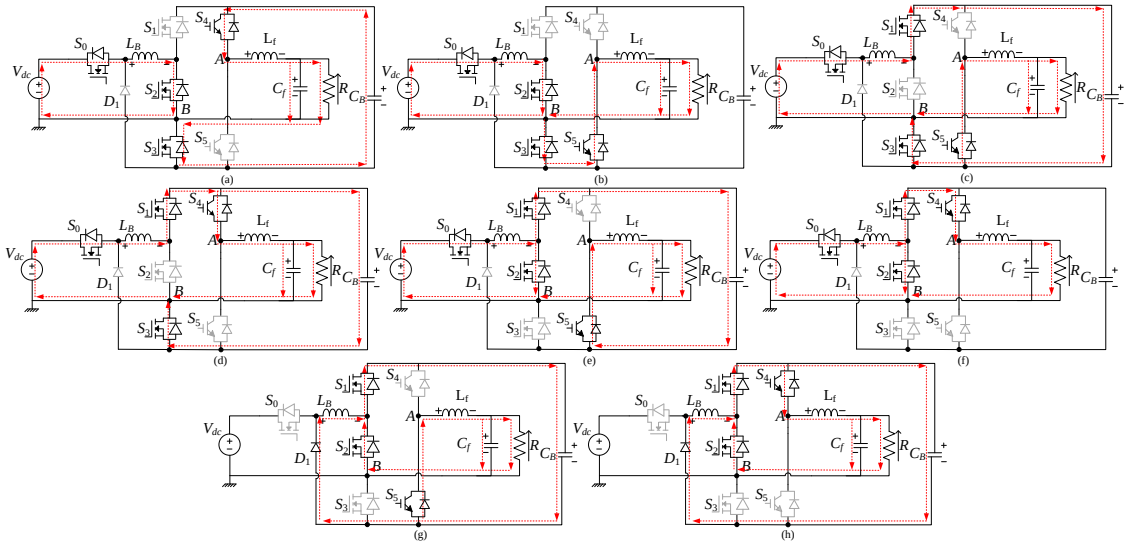


Figure 2. *Operation modes of the proposed 1P-CG-BBI. (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5, (f) Mode 6, (g) Mode 7, (h) Mode 8*

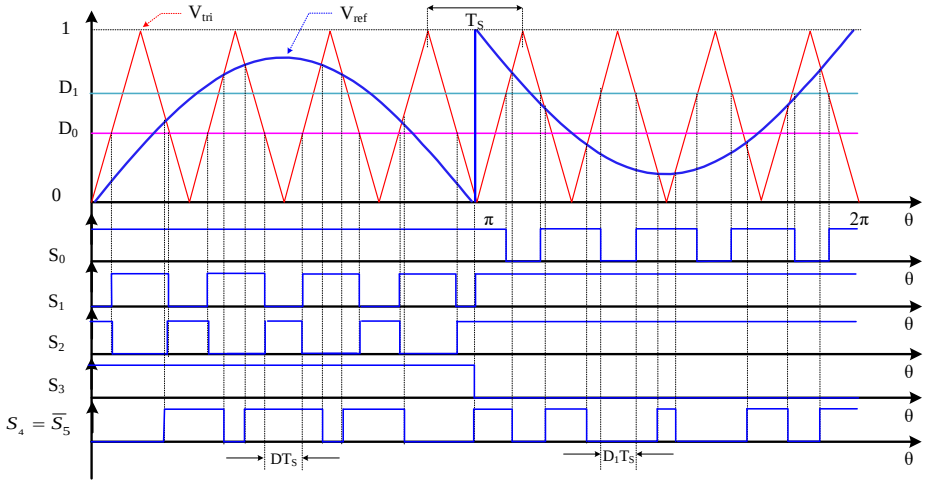


Figure 3. *Proposed PWM method for 1P-CG-BBI.*

In mode 3 and mode 4, switch S_2 is off, and switch S_1 is turned on. The inductor L_B releases energy to the capacitor C_B and the DC-AC section. The voltage across the inductor L_B and the current through capacitor C_B are calculated as follows:

$$\begin{cases} V_{LB} = L_B \dfrac{di_{LB}}{dt} = V_{dc} - V_{CB} \\ I_{CB} = C_B \dfrac{dv_{CB}}{dt} = I_{LB} - I_{PN} \end{cases} \tag{2}$$

During the positive half-cycle, the DC-DC side operates as a boost converter. Therefore, the voltage across the capacitor V_{CB} is calculated as follows:

$$V_{CB} = \frac{V_{dc}}{1 - D_0} \tag{3}$$

Where: D_0 is the duty cycle of switch S_2, $1 - D_0$ is the duty cycle of switch S_1

In the negative half-cycle, modes 5-8 are applied, as shown in Figures 2(e)-2(h). In modes 5 and 6, switch S_0 is closed, diode D_1 is off, and inductor L_B stores energy from the input source V_{dc}. The voltage across inductor L_B and the current through capacitor C_B are calculated as follows:

$$\begin{cases} V_{LB} = L_B \dfrac{di_{LB}}{dt} = V_{dc} \\ I_{CB} = C_B \dfrac{dv_{CB}}{dt} = -I_{PN} \end{cases} \tag{4}$$

In modes 7 and 8, switch S_0 is off, and diode D_1 is gated on. Inductor L_B releases energy to capacitor C_B and the inverter section. The voltage across inductor L_B and the current through capacitor C_B are calculated as follows:

$$\begin{cases} V_{LB} = L_B \dfrac{di_{LB}}{dt} = -V_{CB} \\ I_{CB} = C_B \dfrac{dv_{CB}}{dt} = I_{LB} - I_{PN} \end{cases} \tag{5}$$

It can be observed that, during the positive half-cycle, the DC-DC section operates as a buck-boost converter. Thus, the voltage across capacitor V_{CB} is calculated as follows:

$$V_{CB} = V_{dc} \frac{D_1}{1 - D_1} \tag{6}$$

Where D_1 is the duty cycle of switch S_0.

The voltage across the capacitor V_{CB} is desired to be equal during both the positive and negative half-cycles, so the value of D_1 is calculated for the negative half-cycle as follows:

$$V_{CB} = \frac{V_{dc}}{1 - D_0} = V_{dc} \frac{D_1}{1 - D_1} \Rightarrow D_1 = \frac{1}{2 - D_0} \tag{7}$$

By combining these operating modes, the DC voltage V_{CB} of the proposed 1P-CG-BBI can be boosted from the input voltage, similar to any conventional two-stage inverter. The output voltage V_{AB} of the proposed configuration has a three-level waveform: $+V_{CB}$, 0, $-V_{CB}$, as shown in Table 1.

Table 1. *ON/OFF states of the switching devices*

MODE	Switches						Diode	V_{AB}
	S_0	S_1	S_2	S_3	S_4	S_5	$D1$	
1	ON	OFF	ON	ON	ON	OFF	OFF	$+V_{CB}$
2	ON	OFF	ON	ON	OFF	ON	OFF	0
3	ON	ON	OFF	ON	OFF	ON	OFF	0
4	ON	ON	OFF	ON	ON	OFF	OFF	$+V_{CB}$
5	ON	ON	ON	OFF	OFF	ON	OFF	$-V_{CB}$
6	ON	ON	ON	OFF	ON	OFF	OFF	0
7	OFF	ON	ON	OFF	OFF	ON	ON	$-V_{CB}$
8	OFF	ON	ON	OFF	ON	OFF	ON	0

In the positive half-cycle, the inverter section operates as a single-phase bridge inverter. The output voltage V_{AB} is calculated as follows:

$$V_{AB} = V_{CB} \times V_{ref} = V_{CB} \times M \sin(\theta) \tag{8}$$

Where: $V_{ref} = M \times \sin(\theta)$ is reference voltage of switch S_4, $(1 - V_{ref})$ is reference voltage of switch S_5

In the negative half-cycle, the output voltage V_{AB} of the inverter is calculated as follows:

$$V_{AB} = -V_{CB} \times (1 - V_{ref}) = V_{CB} \times M \sin(\theta) \tag{9}$$

Where: $V_{ref} = 1 + M \times \sin(\theta)$ is reference voltage of switch S_4, $1 - V_{ref}$ is reference voltage of S_5

From equations (8) and (9), the voltage V_{AB} of the proposed 1P-CG-BBI is calculated as follows:

$$V_{AB} = V_{CB} \times m_a \tag{10}$$

With: $m_a = M \times \sin(\theta)$

The peak-value of fundamental harmonic of output voltage V_{AB} is calculated as:

$$V_{AB} = \begin{cases} \dfrac{V_{dc} \times M \sin(\theta)}{1 - D_0}; & (0 \le \theta < \pi) \\ V_{dc} \times M \sin(\theta) \dfrac{D_1}{1 - D_1}; & (\pi \le \theta < 2\pi) \end{cases} \tag{11}$$

The voltage gain G of the inverter is defined as:

$$G = \frac{V_{AB,1^{st}-order,peak}}{V_{dc}} = \frac{M}{1 - D_0} \tag{12}$$

2.2. Component selection

2.2.1. Inductor and capacitor selections

Based on equation (7), we observe that the duty cycle D_1 depends on the duty cycle D_0, and within the range [0,1) is always greater than D_0. This implies that during the negative half-cycle, the current ripple will be larger compared to the positive half-cycle. Based on equation (4), the current ripple ΔI_{LB} of the inductor L_B and the selection of the inductor are determined as follows:

$$\Delta I_{LB} = \frac{V_{dc} D_1 T_S}{L_B} \rightarrow L_B \ge \frac{V_{dc}^2 D_1 (1 + D_1) T_S}{2 k_L \% P_O} \tag{13}$$

The inductor L_B is selected such that $\Delta I_{LB} \le k_L\% \ \bar{I}_{LB,T_O}$, where $k_L\%$ is the maximum current ripple

The capacitance of C_B can be approximated by the following expression:

$$C_B \ge \frac{P_O T_S}{k_C \% V_{AB} \bar{V}_{CB,T_O}} \tag{14}$$

2.2.2. Semiconductor devices selections

The voltage stress on the switch S_0 and diode D_1 of the inverter is equal (V_{dc}+V_{CB}) during the operating modes. The currents through switch S_0 and diode D_1 are equal to inductor current I_{LB}.

The voltage stress on the switch $S_1 - S_5$ is equal to the voltage on the capacitor C_B. The currents through switches $S_1 - S_3$ are equal to inductor current I_{LB}. While switches $S_4 - S_5$ are designed equal to output current $I_O = P_O / V_O$.

2.3. Small-signal analysis

The small-signal analysis of the 1P-CG-BBI is conducted for both the positive and negative half-cycles. The 1P-CG-BBI circuit will be analyzed separately for both the buck-boost DC-DC converter and the half-bridge DC-AC converter.

2.3.1. Small-signal analysis for DC-DC buck-boost converter

In the positive half-cycle, when switches S_0, S_3 are gated off, and the two switches S_1 and S_2 alternately gated on and off according to the modulation ratio d, the following equations can be derived by averaging the state equations (1) and (2):

$$L_B \frac{d\bar{i}_{LB}}{dt} = \bar{v}_{dc} - \bar{v}_{CB}(1-\bar{d}) - r_{LB}\bar{i}_{LB} \tag{15}$$

$$C_B \frac{d\bar{v}_{CB}}{dt} = \bar{i}_{LB}(1-\bar{d}) - \bar{i}_{PN} \tag{16}$$

Assume that any average signal consists of a DC signal X and a small AC signal $\tilde{x}$, and $\bar{x} = X + \tilde{x}$, $\tilde{x} << X$. Substituting into equations (15) and (16), and then applying the Laplace transform to both sides, the following linearized equations are obtained:

$$\tilde{i}_{LB}(s) = \frac{\tilde{v}_{dc}(s) + V_{CB}\tilde{d}(s) - (1-D)\tilde{v}_{CB}(s)}{L_B s + r_{LB}} \tag{17}$$

$$\tilde{v}_{CB}(s) = \frac{(1-D)\tilde{i}_{LB}(s) - I_{LB}\tilde{d}(s) - \tilde{i}_{PN}(s)}{C_B s} \tag{18}$$

In which, $\bar{x}$ represents the average of the signal x.

Based on equations (17) and (18), the transfer functions $G_{C1}(s)$ can be derived as follows.

$$G_{C1}(s) = \frac{\tilde{v}_{CB}}{\tilde{d}}\bigg|_{\substack{\tilde{v}_{dc}=0 \\ \tilde{i}_{PN}=0}} = \frac{(1-D)V_{CB} - I_{LB}L_B s - I_{LB}r_{LB}}{L_B C_B s^2 + r_{LB}C_B s + (1-D)^2} \tag{19}$$

In the negative half-cycle, when switches S_1, S_2 are turned on, switch S3 is turned off, and switch S_0 is switching according to the modulation ratio d_1, by averaging the state equations (4) and (5), the following equations can be obtained:

$$L_B \frac{d\bar{i}_{LB}}{dt} = \bar{v}_{dc}\bar{d}_1 - \bar{v}_{CB}(1-\bar{d}_1) - r_{LB}\bar{i}_{LB} \tag{20}$$

$$C_B \frac{d\bar{v}_{CB}}{dt} = \bar{i}_{LB}(1-\bar{d}_1) - \bar{i}_{PN} \tag{21}$$

Similar to the analysis above, the transfer functions $G_{C2}(s)$ can be derived as follows

$$G_{C2}(s) = \frac{\tilde{v}_{CB}}{\tilde{d}_1}\bigg|_{\substack{\tilde{v}_{dc}=0 \\ \tilde{i}_{PN}=0}} = \frac{(1-D_1)(V_{CB}+V_{dc}) - I_{LB}L_B s - I_{LB}r_{LB}}{L_B C_B s^2 + r_{LB}C_B s + (1-D_1)^2} \tag{22}$$

2.3.2. Small-signal analysis for H-bridge Inverter

The inverter section of the 1P-CG-BBI circuit operates as a single-phase bridge inverter with the input voltage being the voltage across the capacitor C_B.

By averaging the state equation (10), the following equation can be derived:

The transfer functions of the inverter $G_{id}(s)$, $G_{vi}(s)$ are presented through equations (24) and (25).

$$\bar{V}_{AB,T_s} = \bar{V}_{CB} \times \bar{m}_a \tag{23}$$

$$G_{id}(s) = \frac{\tilde{i}_L}{\tilde{m}_a}\bigg|_{\substack{\tilde{v}_c=0\\ \tilde{v}_{CB}=0}} = \frac{\tilde{i}_L}{\tilde{v}_{AB}}\bigg|_{\tilde{v}_c=0} \times \frac{\tilde{v}_{AB}}{\tilde{m}_a}\bigg|_{\tilde{v}_{CB}=0} = \frac{V_{CB}}{Ls + r_L} \tag{24}$$

$$G_{vi}(s) = \frac{\tilde{v}_C}{\tilde{i}_L}\bigg|_{\tilde{i}_R=0} = \frac{1}{Cs} \tag{25}$$

2.4. Controller Design

2.4.1. Designing the PI Controller for the Buck-Boost DC-DC Converter in the 1P-CG-BBI topology

The capacitor voltage V_{CB} is regulated by a PI controller as illustrated in Figure 4. The PI controller is defined as follows:

$$G_{PI} = \left(K_P + \frac{K_I}{s}\right) \tag{26}$$

Figure 5 presents the Bode plot of the transfer functions $G_{C2}(s)$ and $G_{C4}(s)$ referenced in (19) and (22). This Bode plot is constructed for an output power of 302.5W and 100 VDC input source. The capacitor voltage V_{CB} and the output voltage are controlled at 200V and 110V_{rms}, respectively. Based on equations (3), (7), and (13), the coefficients D, $D1$ and I_{LB} are calculated as 0.5, 0.67, and 3.62 A. According to (13) and (14), the values of inductor L_B and capacitor C_B are chosen to be 3 mH and 4 mF, respectively, with the impedance of inductor L_B being 0.3 Ω.

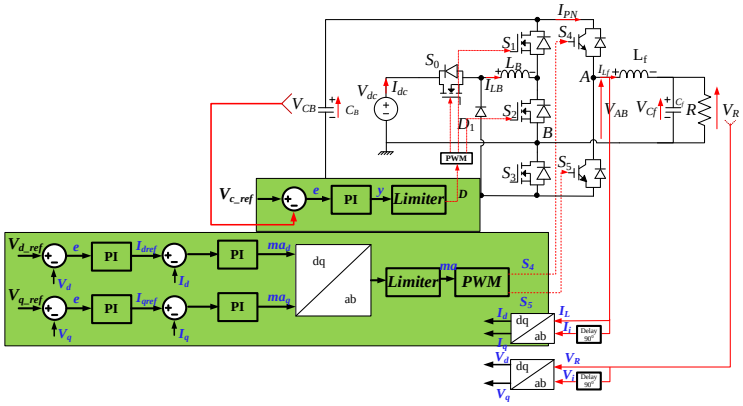
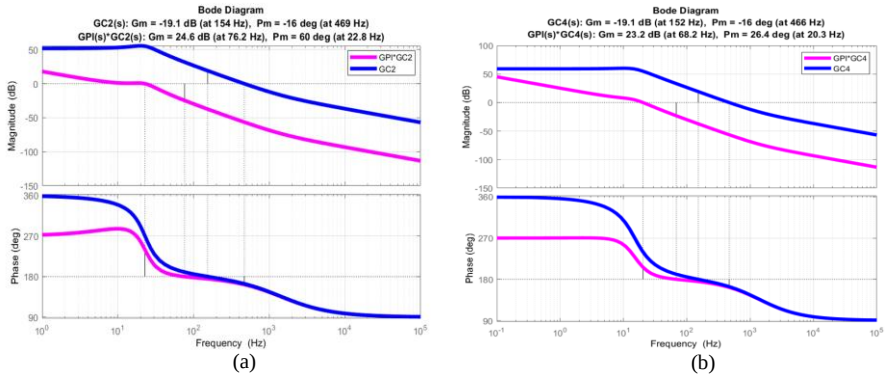


Figure 4. *The Control Block Diagram of the proposed 1P-CG-BBI*



(a) (b)

Figure 5. *Bode diagram of (a) $G_{C2}(s)$, $G_{PI}(s)G_{C2}(s)$ và (b) $G_{C4}(s)$, $G_{PI}(s)G_{C4}(s)$*

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2.4.2. Design of a PI Controller for the DC-AC Inverter Circuit in the 1P-CG-BBI

The dq transformation for a single-phase system is an essential element in the control circuitry of inverter systems [10].

$$\begin{bmatrix} d \\ q \end{bmatrix} = \begin{bmatrix} \sin(\omega t) & -\cos(\omega t) \\ \cos(\omega t) & \sin(\omega t) \end{bmatrix} \begin{bmatrix} a \\ b \end{bmatrix} \tag{27}$$

With a and b being the transformed quantities (output voltage, current through the inductor), the transfer functions on the d and q axes of the system are expressed as follows:

$$G_{idx}(s) = \frac{\tilde{i}_x}{\tilde{m}_{ax}}\bigg|_{\substack{\tilde{v}_c = 0 \\ \tilde{v}_{CB} = 0}} = \frac{V_{CB}}{r_L + sL} \tag{28}$$

$$G_{vix}(s) = \frac{\tilde{v}_{Cx}}{\tilde{i}_x}\bigg|_{\tilde{i}_{Rx} = 0} = \frac{1}{Cs} \tag{29}$$

With (x= d, q)

The modulation index applied to the PWM stage is determined as follows:

$$m_a = m_{ad} \times \sin(\omega t) + m_{aq} \times \cos(\omega t) \tag{30}$$

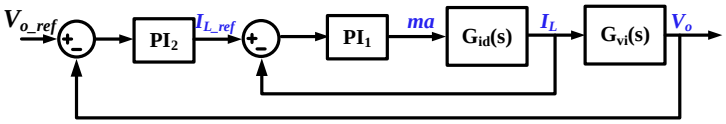
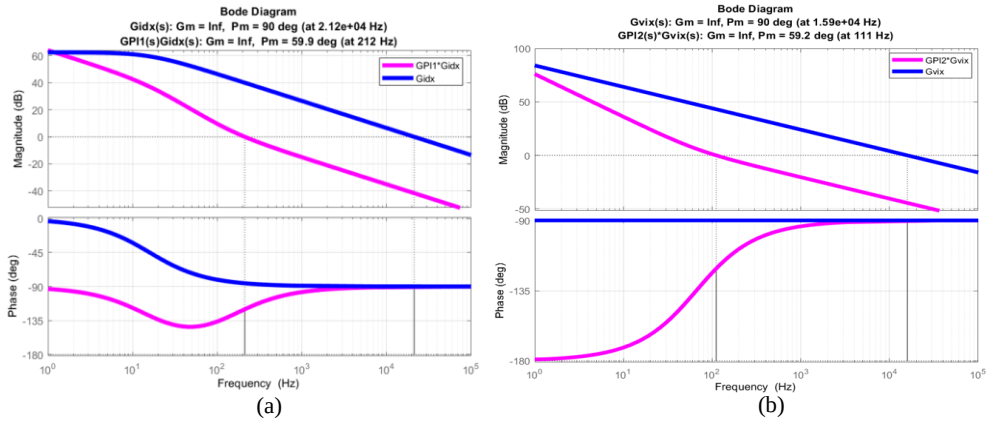


Figure 6. *Controller of DC-AC side*

The PI_1 & PI_2 controller in Figure 6 is defined as follows:

$$G_{PI_1}(s) = \frac{1}{V_{CB}}\left(K_P + \frac{K_I}{s}\right);\ G_{PI_2}(s) = K_P + \frac{K_I}{s} \tag{31}$$



(a) (b)

Figure 7. *Bode diagram of (a) $G_{idx}(s)$, $G_{PI1}(s)G_{idx}(s)$ và (b) $G_{vix}(s)$, $G_{PI2}(s)G_{vix}(s)$*

Figure 7 presents the Bode plots of the transfer functions G_{idx}(s) and G_{vix}(s) as defined in equations (28) and (29). Based on the Bode plot in Figure 7, it can be observed that before adding the PI controller, the system has a gain margin (Gm) of infinity and a phase margin (Pm) of 90°, both of which are greater

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than zero. Although the system is stable according to Bode's criterion [11], the crossover frequency (ω_c) is excessively high, making the system more sensitive to high-frequency disturbances. After introducing the PI controller, the adjusted crossover frequency (ω_c) is reduced, allowing the system to filter out disturbances above the cutoff frequency. As a result, the system becomes more stable.

3. Overall comparison study

Table 2. *Overall comparison study*

	Inverter in [12]	Inverter in [13]	Boost + 3L-ANPC [14]	1P-CG-BBI
D and M	$D \geq M$	$D \geq 2M-1$	Decoupled	Decoupled
Boost factor, B	$1/(1-D)$	$1/(1-D)$	$1/(1-D)$	$1/(1\text{-}D_0)=D_1/(1\text{-}D_1)$
Voltage gain, G	MB	MB	MB/2	MB
Capacitor voltage rating, V_C/V_{dc}	B	B for C_1, B/2 for C_2	B/2	B
Switch voltage rating, V_S/V_{dc}	B	B for S_1 - S_5, B/2 for S_6, S_7	B for boost switch, B/2 for inv. switch	B+1 for S_0 B for S_1 - S_5
Diode voltage rating, V_D/V_{dc}	NA	NA	B	B+1 for S_0 B for S_1 - S_5

As shown in Table 2, all topologies use the same number of inductors, including one boost inductor. The proposed 1P-CG-BBI and the inverter in [12] need only one, while the inverter in [13] and the 3L-ANPC inverter in [14] require two capacitors for AC output. Although the proposed inverter uses one additional switch compared to [12], it decouples the duty ratio D and modulation index M, allowing M to reach 1, independent of D. This enables higher M, lower DC-link voltage, and reduced component voltage ratings, offering superior performance.

The efficiency of the 1P-CG-BBI is compared with the topology in study [12] using the PLECS simulation software. For the proposed configuration, the semiconductor switches used on the inverter side are IKWH30N65WR6 with a voltage rating of 650V, while the IGBTs used on the DC-DC side are IKW50N120CS7 with a voltage rating of 1200V. All the switches in the configuration of study [12] are IGBTs of type IKW50N120CS7, with a voltage rating of 1200V.

It can be observed that the proposed configuration achieves higher efficiency compared to the configuration in [12] within the power range of 300W-1kW, as is presented in Figure 8.

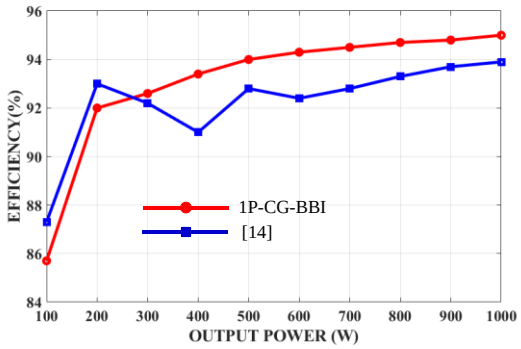

Figure 8. *The efficiency of the 1P-CG-BBI and the topology in [12].*

4. Experiment results

The proposed inverter configuration has been verified through experiments. The parameters for the experiments are listed in Table 3.

Table 3. *Experiment parameters*

Parameters	Symbol	Value
Input voltage	V_{dc}	100V
Output voltage	V_o	110Vrms
Switching frequency	f_s	10kHz
Switches	S_0-S_3	AIMW120R080M1(1200V, $R_{DS(on)}$ = 80mΩ)
Switches	S_4-S_5	IHW20N65R5 (650V, $V_{CE(sat)}$ = 1.35V)
Diode	D_1	IDP18E120 (1200V, V_F = 1.65V)
Load	R	40Ω

The experiment was conducted using a 300-W model in the laboratory. The experimental parameters are listed in Table 3. The DSP TMS320 F28379D microcontroller was used to control the inverter. The experimental model of the proposed 1P-CG-BBI inverter is presented in Figure 9, and the experimental results of the proposed inverter are shown in Figures 10, 11, 12, and 13. In Figures 10(a) and 10(b), the capacitor voltage is controlled at 200V. The RMS value of the output load voltage is 110- V_{RMS}, as shown in Figure 10(a). The RMS value of the output load current is 2.76 A_{RMS}, also shown in Figure 10(a).

In Figures 10(c), 10(d), and 10(e), the gate voltage of switches V_D, S_0 is the sum of V_{in} and the peak absolute value of V_{CB}, while the gate voltage of switches S_1, S_2 is the peak absolute value of V_{CB}. The gate voltage of switches S_3, S_4, S_5 is also the peak absolute value of V_{CB}, as shown in Figures 10(f), 10(g), and 10(h). The laboratory prototype achieves an output power of 300W with an input voltage of 100V.

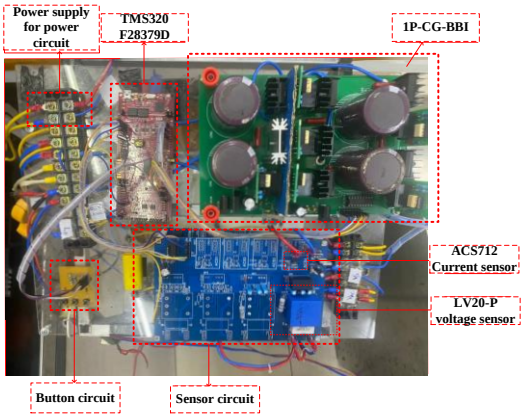

Figure 9. *Prototype of 1P-CG-BBI topology.*

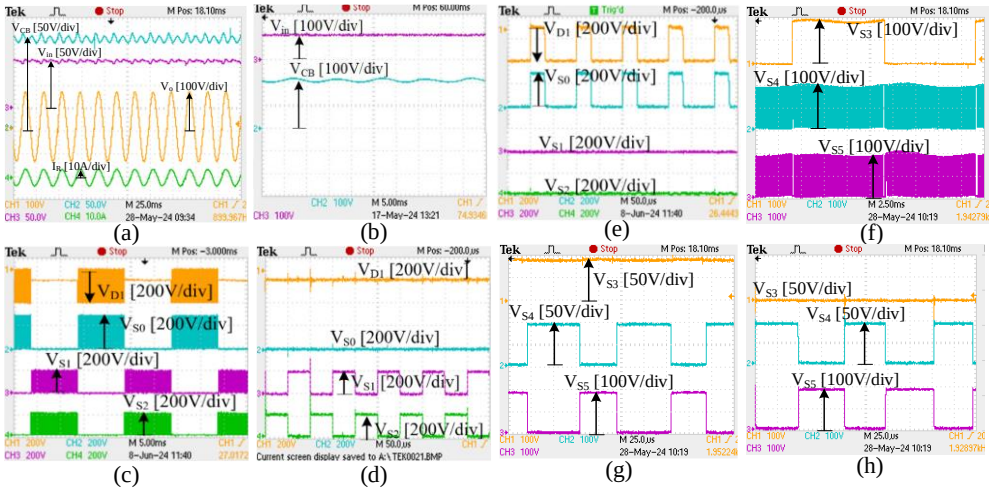

Figure 10. *The experimental results at an input voltage level of 100V*

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With an input voltage of 80V, the voltage on the DC-DC side is controlled at 200V, and the voltage on the inverter side is controlled at 140V_{PEAK} (equivalent to 100 V_{RMS}). After increasing the input voltage from 80V to 110V, as shown in Figures 11(a) and 11(c) and then decreasing it back from 110V to 80V, as shown in Figures 11(b) and 11(d), the voltage across the capacitor remains approximately at the set value of 200V, specifically 202V, and the output voltage stays around the set value of 140V_{PEAK}, specifically 139 V_{PEAK}.

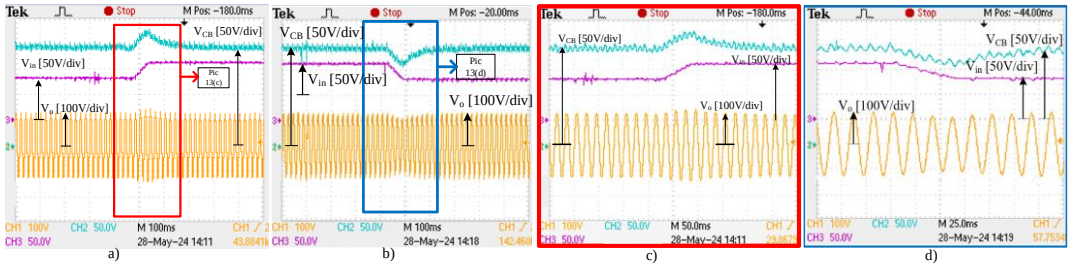

Figure 11. *Experiment results of changing input voltage value*

Testing the capability of controlling the DC-DC voltage by keeping the input voltage V_{in} constant at 100V, with the inverter output voltage set to 145 V_{PEAK}, involves changing the DC-DC voltage from 190V to 210V, as shown in Figures 12(a) and 12(c) and then back to 190V, as shown in Figures 12(b) and 12(d). During this process, it was observed that the input voltage remained constant at the initially measured value of 102.4V, and the output voltage on the load was maintained at approximately the set value of 145 V_{PEAK}, with a measured value of 147 V_{PEAK}.

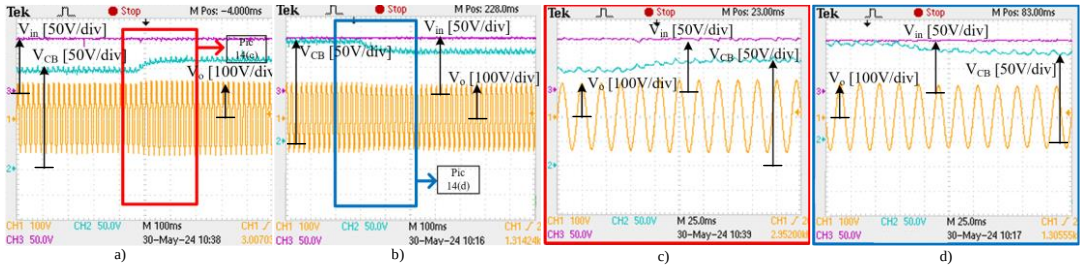

Figure 12. *Experiment results of changing capacitor voltage value C_B*

Testing the capability to control the inverter-side voltage involves keeping the input voltage constant at 100V, with the DC-DC voltage set to 200V. The peak voltage on the inverter side is adjusted from 100 V_{PEAK} to 143 V_{PEAK}, as shown in Figures 13(a) and 13(c) and then back from 143 V_{PEAK} to 100 V_{PEAK}, as shown in Figures 13(b) and 13(d). During this test, it was observed that the input voltage remained constant at the initially measured value of 102.4V, and the voltage across the capacitor remained nearly unchanged at 201V.

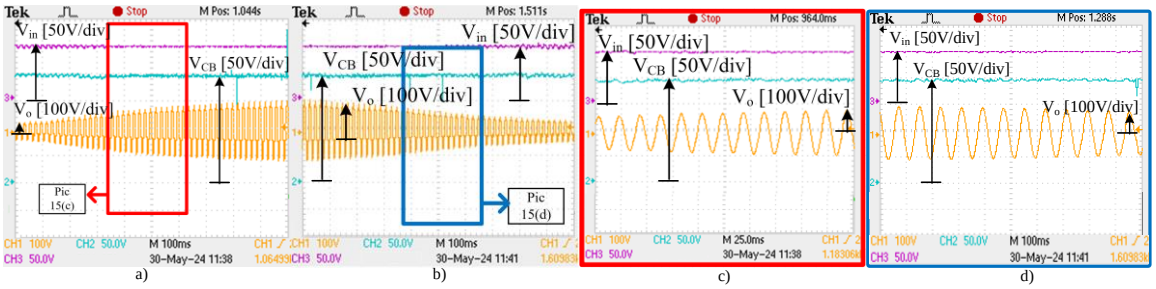

Figure 13. *Experiment results of changing output voltage value*

5. Conclusions

The paper proposes and analyzes a new single-phase inverter configuration, the Common Ground (CG) Buck-Boost configuration, which is capable of eliminating common-mode voltage (CMV). It has achieved significant results, with the Common Ground configuration effectively eliminating CMV. The

application of a PI controller allows for the adjustment of voltage in both DC-DC and DC-AC operations. Results from simulations and experiments demonstrate that the system achieves high stability and significantly improves energy conversion efficiency, reducing energy losses and enhancing overall performance. This research not only addresses the limitations of traditional common ground systems but also opens new pathways for applications requiring high performance and stability, particularly in renewable energy applications.

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Conflict of Interest

The authors declare no conflict of interest

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