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Four-Level Neutral Point Clamped Inverter Fed by 18-Pulse Diode Rectifier With Low Input and Output Harmonic Distortion

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ABSTRACT

The four-level neutral point clamped (4L-NPC) inverter is a common and cost-effective topology among four-level inverters. However, balanced DC voltage sources at the input are necessary to ensure output quality. Therefore, this paper introduces a simplified power conversion system that includes an 18-pulse diode rectifier designed to supply the 4L-NPC inverter while significantly reducing harmonic distortion on both the input and output sides. The system employs an 18-pulse rectifier configuration to lower the harmonic content at the input and ensure a balanced DC voltage for the 4L-NPC inverter, thereby improving the quality of the output waveform. The combined system effectively reduces harmonic distortion on both the input and output sides, enhancing overall performance for industrial applications. Simulation results validate the system's ability to reduce Total Harmonic Distortion (THD) on the input while maintaining superior output performance from the 4L-NPC inverter. This approach provides an effective solution for high-power applications where controlling harmonic distortion is essential to meet strict power quality standards.

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1. Introduction

Multilevel inverters have attracted considerable attention as potential alternatives to traditional two-level inverters in medium-voltage and high-power applications due to their enhanced output quality and better efficiency performance [1], [2]. The three-level neutral point clamped (3L-NPC) inverter is particularly popular in industry for various applications across different voltage ranges, owing to its simple power stage configuration. However, the increasing demand for medium voltage and high power in commercial and industrial sectors has sparked greater interest in higher-level multilevel inverters. The four-level neutral point clamped (4L-NPC) inverter, for example, can operate at higher voltages with reduced device voltage ratings, lower switching losses due to lower switching voltage, improved harmonic performance, and smaller grid filters compared to three-level inverters [3].

The 4L-NPC inverter is a common and cost-effective topology among four-level inverters. However, it suffers from a significant neutral point (NP) voltage imbalance problem. This issue can be addressed through software-based modulation schemes using virtual vectors or multi-pulse switching, which can lead to increased switching losses, higher common-mode voltage, and inferior output waveform quality [4]–[8].

Fortunately, the 4L-NPC inverter can achieve DC voltage balancing through hardware-based solutions [9]–[12]. For instance, in grid-tied photovoltaic (PV) 4L-NPC inverters, front-end DC-DC converters can help enhance MPPT, ensure balancing, and boost the DC voltage [9], [10]. Besides, isolated front-end multi-pulse diode rectifiers offer benefits for high-power, medium-voltage multilevel NPC converters, enabling low total harmonic distortion (THD) of the AC input current and a high-power factor [2], [11], [12]. In numerous industrial applications, the 18-pulse rectifier system is regarded as a cost-effective solution for reducing harmonic distortion in the input current. Additionally, the 18-pulse

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rectifier offers superior rectification characteristics compared to 12-pulse rectifiers while featuring a simpler structure than 24-pulse rectifiers [13].

Therefore, this paper proposes a simplified and low-cost solution applied in an electric drive system that consists of a Four-Level Neutral Point Clamped (4L-NPC) inverter fed by an 18-pulse diode rectifier, designed to achieve low input and output harmonic distortion. The proposed system utilizes an 18-pulse rectifier configuration, which is expected to reduce the harmonic content at the input side and ensure the balanced DC voltage of the capacitor input for the 4L-NPC inverter to enhance the output waveform quality. The structure of the paper is as follows: Section 2 describes the configuration of the proposed system, Section 3 presents the simulation results to validate the system's performance, and Section 4 contains the discussions.

2. Four-Level Neutral Point Clamped Inverter Supplied from Isolated Front-end 18-Pulse Diode Rectifiers

2.1. Four-Level Neutral Point Clamped Inverter Topology

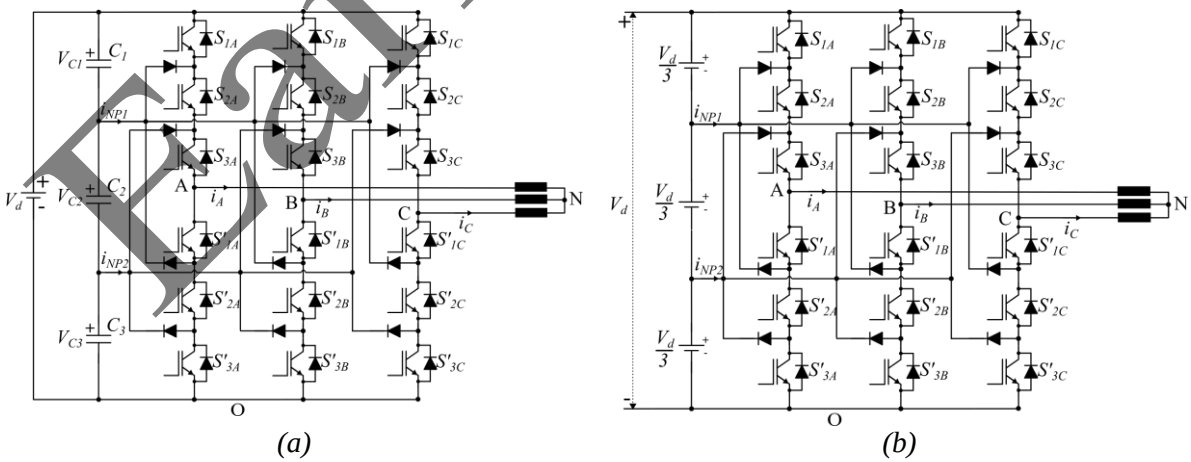
Fig. 1 shows a schematic diagram of a three-phase four-level neutral point clamped (4L-NPC) inverter. The three-phase legs share a common DC-link with a total voltage of V_d. Depending on the availability of DC sources or specific applications [14], the DC-link in a 4L-NPC inverter can be configured in two ways: with a single DC source or with separate DC sources, as shown in Fig. 1. Each phase of the inverter has six switches in complementary operation (S_{1X}, S'_{1X}), (S_{2X}, S'_{2X}), (S_{3X}, S'_{3X}), (where X = A, B, and C), and the clamping diodes. The switching function of each phase S_X is defined as:

$$S_X = \sum_{i=1}^{3} S_{iX} = S_{1X} + S_{2X} + S_{3X} \tag{1}$$

Under the DC voltage balance, the output phase voltage is:

$$\begin{bmatrix} V_{AO} \\ V_{BO} \\ V_{CO} \end{bmatrix} = \frac{V_d}{3} \begin{bmatrix} S_A \\ S_B \\ S_C \end{bmatrix} \tag{2}$$

Based on (2), the 4L-NPC inverter generates four levels of output phase voltage depending on the switching state function: 0, $V_d/3$, $2V_d/3$, and V_d, in which, V_d is the total DC-link voltage.



(a) *(b)*

Figure 1. *Four-Level Neutral Point Clamped Inverter with (a): single DC source; (b): separate DC sources.*

Table 1. *Switching states of 4L-NPC inverter*

S_X	S_1	S_2	S_3	i_{NP1}	i_{NP2}	v_{AO}
0	0	0	0	0	0	0

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1	0	0	1	i_X	0	$V_d/3$
2	0	1	1	0	i_X	$2V_d/3$
3	1	1	1	0	0	V_d

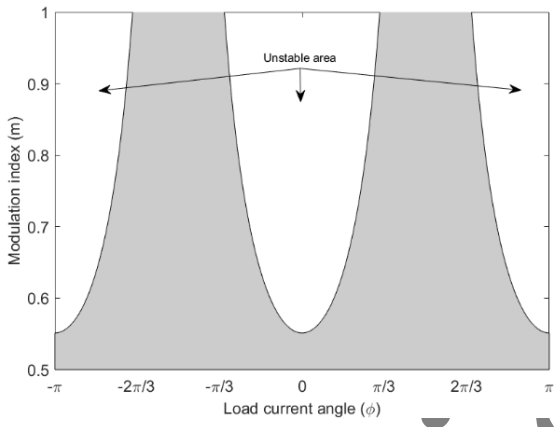

Figure 2. *Voltage balancing limits of 4L-NPC inverter.*

Table 1 shows the relationship between switching function S_X, switching states (S_1, S_2, S_3), output voltage (v_{AO}), and neutral point currents [i_{NP1} i_{NP2}], where i_X represents the three-phase output currents i_A, i_B, or i_C. To maintain voltage balance in the DC-link capacitors of a 4L-NPC inverter with a single DC source, an appropriate choice of redundant switching states can be made in conventional PWM by using the nearest three vectors to set the neutral point currents to zero. However, this method is effective within a limited range of load power factors and modulation indexes, as illustrated in Fig. 2 [15], [16].

2.2. An 18-Pulse Diode Rectifier Fed 4L-NPC Inverter

The multi-pulse diode rectifiers, which are widely used in medium-voltage drive systems, are known to be the main contributors to generating harmonics on both the AC and DC sides. For medium-voltage drive systems, some researchers have proposed AC-DC converter designs with 12-pulse rectifiers. Compared to the six-pulse rectifier, the 12-pulse rectifier offers a significant reduction in the total harmonic distortion (THD) of the line current. However, the THD of the line current in the 12-pulse rectifier still does not meet the harmonic limits specified by IEEE Standard 519-1992 [17]. As a result, a lineside filter is typically needed in practice to further reduce the line current THD. In applications with strict requirements for grid THD quality, the 18-pulse rectifier is a promising solution due to its ability to cancel out lower-order harmonics.

The block diagram of an 18-pulse diode rectifier is shown in Fig. 3. This rectifier consists of three identical six-pulse diode rectifier units, each powered by a phase-shifting transformer with a typical phase displacement between adjacent secondary windings. In general, the phase-shifting angle of a p-pulse diode rectifier is:

$$\delta = 360° / p \tag{3}$$

From (4), the phase-shifting angle is 20° for 18-pulse diode rectifier.

The transformer winding is symbolized by the letter "Y," which indicates a three-phase wye-connected winding, whereas "Z" represents a three-phase zigzag-connected winding. The typical phase displacement values between the primary and secondary line-to-line voltages (denoted as delta) are 20°, 0°, and -20° for the top, middle, and bottom secondary windings, respectively. The inductance L_s represents the total line inductance, while L_l refers to the total leakage inductance of the transformer as seen from the secondary side. For the DC side connection, the output of the 18-pulse diode rectifier can be series-connected and directly linked to the DC filter capacitor. This filter capacitor is assumed to be large enough to ensure that the DC voltage V_d remains ripple-free, providing a single DC source to the

4L-NPC inverter, as depicted in Fig. 1(a). However, this configuration, as mentioned, cannot fully control the capacitor balancing using conventional NTVs PWM techniques. To address the capacitor voltage balancing issue, the outputs of the 18-pulse diode rectifier will be supplied separately to the three capacitors of the 4L-NPC inverter, as shown in Fig. 4. This configuration not only ensures harmonic cancellation at the input but also maintains low Total Harmonic Distortion (THD) on the inverter side by providing a balanced DC supply to the 4L-NPC inverter.

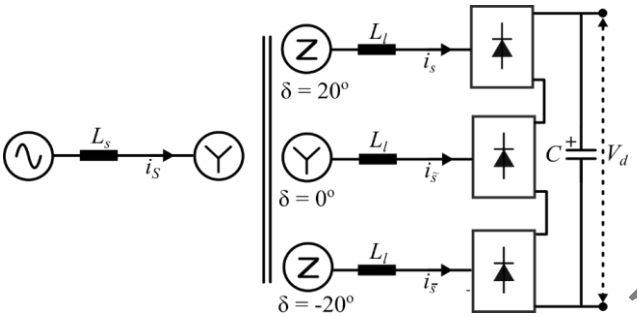

Figure 3. *Block diagram of an 18-pulse diode rectifier.*

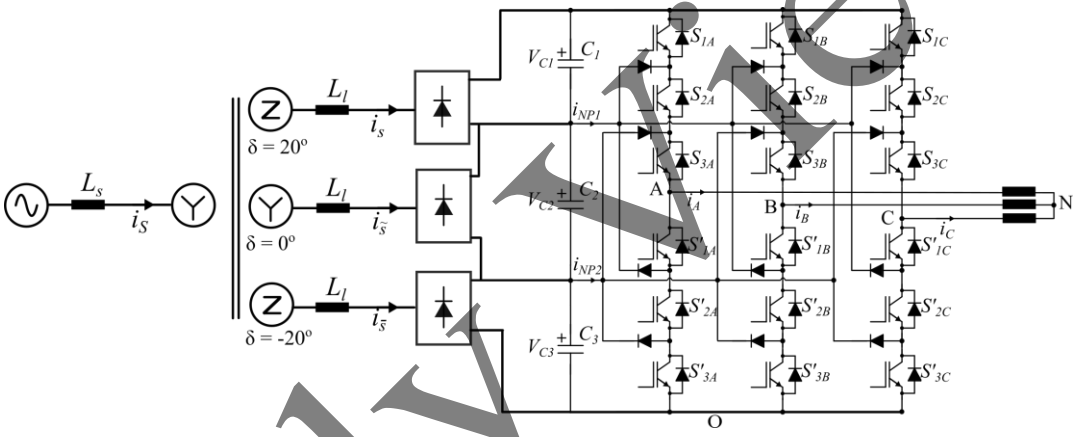

Figure 4. *The proposed diagram of the 18-Pulse Diode Rectifier Fed 4L-NPC Inverter.*

3. Simulation results

In this section, simulation of the system under study is carried out by the PLECS simulation platform. The parameters for simulation include the inverter side and the AC-DC 18-pulse diode rectifier side as shown in Table 2. For the 4L-NPC inverter, the switching pulses are generated using the IPD-SPWM technique. The rated condition is specified when the inverter operates with a modulation index of 0.86.

3.1. Output DC voltage

The voltage waveforms of the DC capacitors are presented in Fig. 5 for different operating conditions: 50% load, 75% load, and full load. In all conditions, the waveforms display a balanced DC voltage with very minute ripples across the three capacitors, demonstrating the advantages of the 18-pulse rectifier.

3.2. Output inverter side

When the capacitor voltages are balanced, the output quality of the 4L-NPC inverter is ensured. This is demonstrated through the waveforms of the output line voltage and the output phase current under different operating modes, as shown in Fig. 6. The Total Harmonic Distortion (THD) of these waveforms is shown in Fig. 7. At nominal operating conditions, the THD for line voltage and phase current are 23.6% and 0.62%, respectively. When operating under sub-nominal loads, the THD values increase. For example, at 50% of the nominal load, these values rise to 31.9% for voltage and 0.83% for current.

3.3. Input line current

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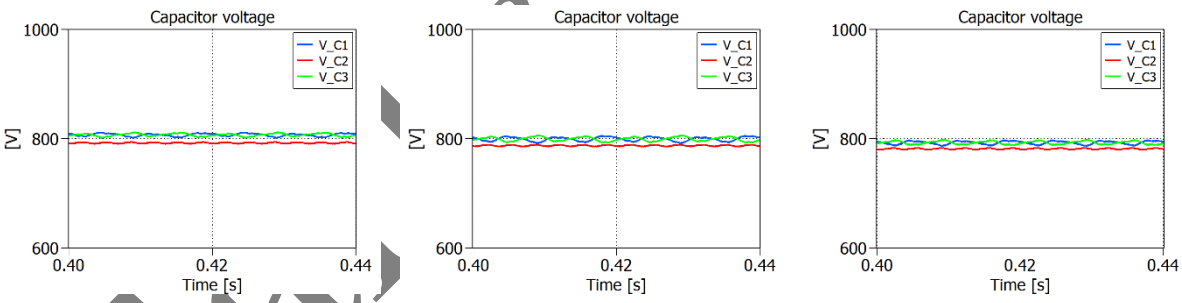
Fig. 8 shows the simulated input secondary current and input line current waveforms at different load conditions when the total line inductance (L_s) is ignored. Under full load conditions, the input line current in Fig. 8(c) closely resembles a pure sinusoidal waveform, with only small values of the 5th, 7th, 11th, and 13th current harmonics, as shown in Table 3. As a result, the Total Harmonic Distortion (THD) of the input line current is only 5.0%.

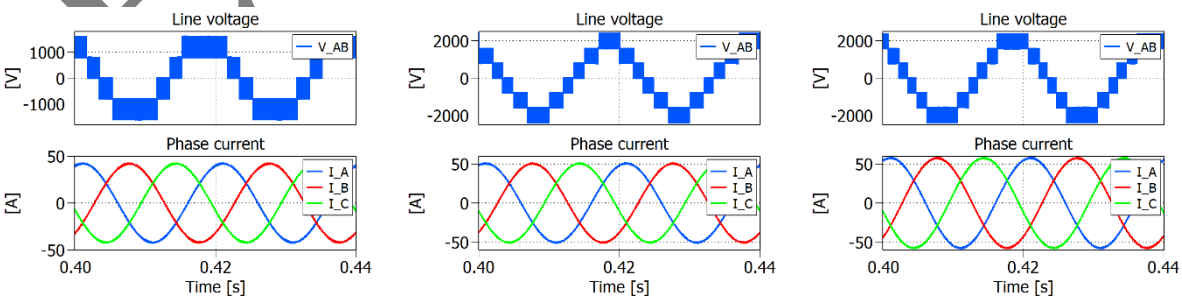
Table 2. *Simulation parameters*

	Parameter	Value
Inverter side	Rated load power (P_n)	100 kW
	Load resistance, inductance (R, L)	4.2 Ω, 4.36 mH
	Capacitance (C)	4700 uF
	Load power factor (PF)	0.95
	Modulation index (m)	0.86
	Carrier frequency	5 kHz
AC-DC side	Total DC-link voltage (V_d)	2400 V
	Separated DC voltage (V_d/3)	800 V
	Leakage inductance (L_l)	1.48 mH
	Main AC line-line input voltage	1825 V
	Transformer ratio	3:1
	Grid frequency	50 Hz



(a) *(b)* *(c)*

Figure 5. *Voltage waveforms of the DC capacitors. (a): at 50% load; (b): at 75% load; (c): at full load*



(a) *(b)* *(c)*

Figure 6. *Output line voltage and phase current of 4L-NPC inverter. (a): 50% load; (b): 75% load; (c): full load*

Under the sub-nominal loads, the imbalance in the currents between the capacitors leads to unbalanced currents in the three secondary windings, as shown in Figs. 8(a) and 8(b). This results in

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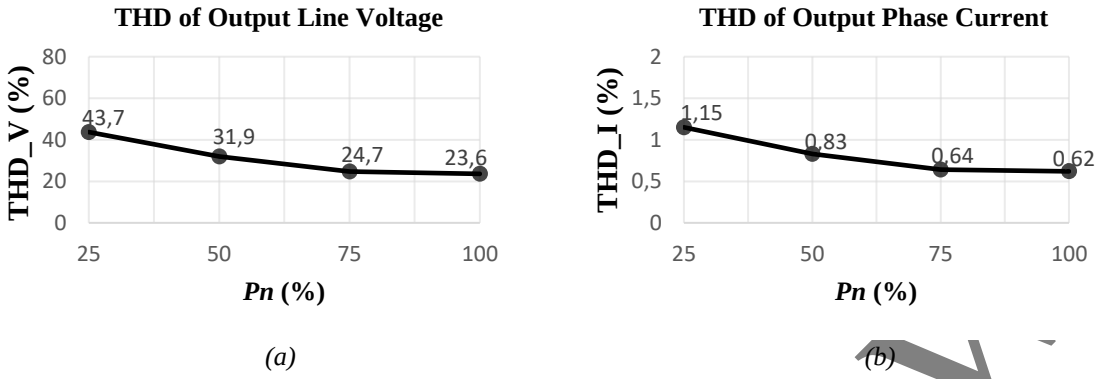
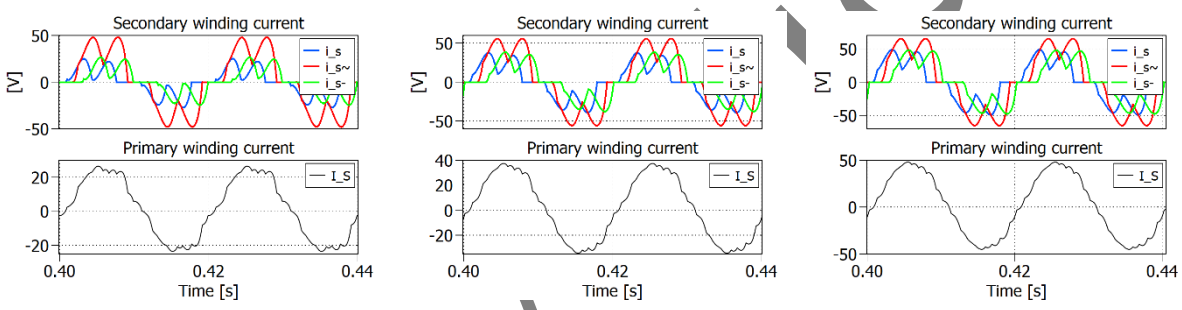
ineffective harmonic cancellation, causing an increase in the 5th, 7th, 11th, and 13th current harmonics, which in turn raises the THD of input line current, as shown in Table 3. For example, at 50% load, the THD of the current increases to 27%.



(a) *(b)*

Figure 7. *Total Harmonic Distortion (THD) of the output line voltage and phase current of a 4L-NPC inverter in relation to operating power.*



(a) *(b)* *(c)*

Figure 8. *Secondary current and input line current when L_s = 0. (a): 50% load; (b): 75% load; (c): full load*

Table 3. *Harmonic content and THD of input line current*

Harmonics (n)	**5**	**7**	**11**	**13**	**THD$_I$ (%)**
i_S *(A)* (25% P_n)	3.1	1.4	1.1	0.7	27.0
i_S *(A)* (50% P_n)	1.8	1.2	0.8	0.6	10.3
i_S *(A)* (75% P_n)	1.5	1.0	0.6	0.5	6.6
i_S *(A)* (100% P_n)	1.4	0.9	0.6	0.5	5.0

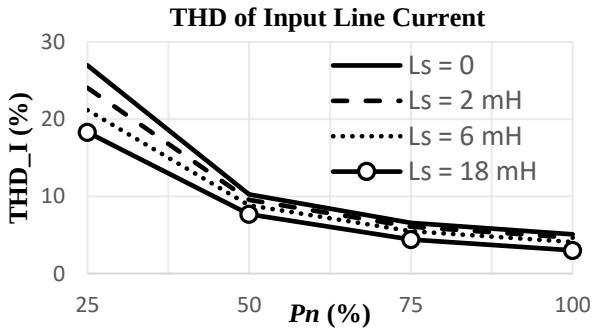


Figure 9. *THD of input line current considering the impact of line inductance L_s*

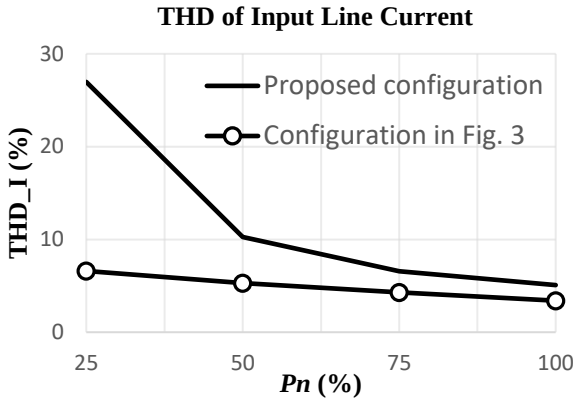


Figure 10. *Comparison of the THD in the input line current between the proposed configuration and the configuration shown in Fig. 3.*

Fig. 9 shows the THD of input line current versus the operating load, with L_s as a parameter. A higher load and higher inductance lead to a lower THD of input line current. For example, with an inductance of 18 mH, the THD at full load is under 3%.

Disregarding the capacitor voltage balancing, the input line current THD of the proposed configuration is compared with that of an 18-pulse rectifier arrangement, where the rectifier outputs are connected in series, as shown in Fig. 3, under the same simulated load power as in the previous tests. In this configuration, the rectifier outputs are connected in series, making the secondary currents of the transformers similar, thus maximizing the harmonic cancellation effect and fully eliminating the 5th, 7th, 11th, and 13th harmonic contents of the input current. Consequently, the input current THD is significantly lower compared to the proposed configuration, as shown in Fig. 10. Under full-load conditions, the input current THD is 3.4% compared to 5% for the proposed configuration. The THD of the input current under lighter loads is also lower than that of the proposed configuration. While the proposed configuration results in a higher input line current THD, it still maintains a THD of under 5% during nominal operation (which is suitable for industrial applications) when L_s = 0, with the potential for further reduction with the addition of an input filter. Additionally, this configuration helps achieve voltage balance across the capacitors of the 4L-NPC inverter, thus ensuring a low output current THD.

4. Conclusion

This paper proposes a simplified power conversion system featuring an 18-pulse diode rectifier that supplies power to a four-level neutral point clamped (4L-NPC) inverter, significantly reducing harmonic distortion at both the input and output. The proposed scheme effectively reduces harmonic distortion on both input and output current, improving overall performance of the system for industrial applications. Simulation results demonstrate that the DC voltage generated by the rectifier is nearly free of ripple, providing a stable and balanced DC source for the 4L-NPC inverter. As a result, the output current THD remains low. While the input line current THD of the proposed system is higher compared to the series-type 18-pulse rectifier, it still maintains a THD below 5%, ensuring its suitability for industrial applications under rated conditions.

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Conflict of interest

The authors declare no conflict of interest in this paper.

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