JTE HCMUTE
ISSN: 2615-9740

JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Education
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

Single-Phase 4-Switch Current-Fed Inverter With Eliminate Leakage Current

Duc Tri Do[1], Bich Nga Truong Thi[1], Tan Hung Nguyen[2*]
[1]Ho Chi Minh City University of Technology and Education, Vietnam
[2]FPT University, Vietnam

*Corresponding author. *Email: hungnt169@fe.edu.vn*

ARTICLE INFO

Received: 15/01/2025
Revised: 13/02/2025
Accepted: 23/06/2025
Published online: 03/11/2025

KEYWORDS

Current-fed Inverter;
Common-Ground;
Boost Inverter;
Leakage Current;
Switched Inductor.

ABSTRACT

This paper introduces a single-phase current-fed inverter topology that enhance output voltage gain, eliminates leakage current, and reduces the number of active switches compared to conventional topology. Leakage current arises from high-frequency common-mode voltage in earlier single-stage boost inverters lacking electrical isolation. Moreover, traditional inverters face challenges in achieving grid amplitude AC output voltage due to their inherent step-down nature. To address these challenges, this study proposes an inverter configuration utilizing four active switches, two diodes, one capacitor, and an impedance source network Type-II, which incorporates three diodes and two inductors to enhance voltage gain. The configuration is connected in a common-ground arrangement between the output load and the input power source, thereby eliminating leakage current. In order to minimize the DC offset, the buffer network employs a single capacitor and makes sure the inverter operates symmetrically for both half-cycles of the AC output. Additionally, this proposed topology is well-suited for PV applications since it uses an appropriate PWM algorithm to regulate the operation of one of the four active switches in both shoot-through and normal modes. This study will provide clarity on the steady-state operating principle analysis. The study's contribution will also be evaluated, and its results will be examined.

Doi: https://doi.org/10.54644/jte.2025.1788

1. Introduction

Recently, alongside traditional energy sources such as hydropower and coal-fired power, solar energy (PV) has been extensively harnessed due to its high efficiency and environmentally friendly characteristics [1]. The Voltage Source Inverter (VSI) is essential for converting DC power to AC. However, since the AC voltage amplitude produced by a VSI is typically lower than the input DC voltage, additional boost circuits or transformers are needed, reducing efficiency and increasing size and cost [2]. To address this, Impedance Source Inverter (ISI) configurations have been proposed, which are suitable for medium and small loads and can operate under short-circuit conditions (ST), thereby improving reliability [3].

Z-Source Inverter (ZSI) and quasi-Z-Source Inverter (qZSI) topologies, which use an impedance source network between the DC source and the inverter, attempt to increase inverter system performance by increasing the DC-Link voltage, as shown in [4], [5]. While these configurations achieve improved functionality, ZSI has a significant limitation of discontinuous input current, causing substantial current ripple and reducing the lifespan of the power source. On the other hand, qZSI addresses the issue of discontinuous input current but requires more components, such as capacitors and inductors, which leads to increased size, weight, and system cost. To overcome these limitations, the Switched Boost Inverter (SBI) proposed in [6] and the Current-Fed Switched Inverter (CFSI) in [7] introduced important advancements. These topologies greatly decrease the amount of passive components in the impedance source network, while maintaining the advantages of ZSI and qZSI, such as increased voltage gain and resilient performance under short-circuit situations. SBI employs a flexible switching mechanism to achieve higher voltage gain with fewer components, whereas CFSI stands out with its continuous input current, which improves system reliability. However, both SBI and CFSI require additional power

switches to support their functionality, which significantly increases power losses and system costs. This becomes a major drawback, especially for systems that demand stable and efficient operation in small- or medium applications. To address these issues, the study in [8] proposed a new ISI configuration that inherits the key advantages of CFSI but is optimized to significantly reduce power losses. This topology uses fewer active and passive components, lowering costs and improving overall efficiency. However, its main drawback is the relatively low voltage gain, which makes it less competitive for applications requiring higher voltage levels.

The ISI topology mentioned above lack electrical isolation between the DC-DC and DC-AC stages, that resulting in the generation of high-frequency common-mode voltage (CMV) across the parasitic capacitance of the photovoltaic (PV) system. This CMV leads to leakage current (i_{LK}), which in turn causes electromagnetic interference (EMI), negatively impacting the system's lifetime and efficiency [9]. To address this problem, studies in [10], [11] proposed H6 and H10 configurations, which help reduce i_{LK} to 45mA and 11.3mA, respectively, ensuring compliance with IEEE 1547 and IEC 61727 standards. Additionally, [12] presents the Common Ground Inverter (CGI) configuration, which effectively eliminates leakage current by using a common ground connection between the load and the PV system. However, these configurations, including H6, H7, and CGI still have a limitation: their AC output voltage amplitude is lower than the input DC voltage amplitude. Therefore, a DC-DC boost converter is required at the front end to boost the voltage to meet the needs of high-voltage loads.

The combination of CGI topology and ISI, known as CG-ISI, has been proposed to increase voltage gain [13], [14]. However, the main problem with this approach is the need for many passive components, which increases the system's size and cost, making it less ideal for cost-sensitive or compact applications. To solve this, [15], [16] introduced a modified CG-ISI structure with fewer passive components, reducing both size and cost. However, this change causes the input current to become discontinuous, which can lower efficiency and cause instability in certain conditions. In [17], a new CG-ISI design with five power switches was studied. This version uses just two impedance elements and fixes the DC offset issue by ensuring symmetrical operation during both the positive and negative cycles of the AC output, which improves performance. However, adding an extra power switch increases switching losses, reducing efficiency, and the additional components make the design more complex and expensive. In [18], four actived switches current-fed topology with common-ground capability was presented, but the voltage gain was still low.

This paper presents an improved topology aimed at enhancing performance and stability in switching circuits. The structure includes four power switches, two diodes, one capacitor, and a Type-II impedance network (Switched-Inductor) with three diodes and two inductors. Using a common-ground configuration, the design effectively eliminates leakage currents and reduces noise. A key feature is the decoupling capacitor, which stabilizes the system, minimizes DC offset, and improves energy efficiency by reducing switching losses. The control system employs PWM to regulate the active switches allowing operation in all modes, optimizing performance for solar energy applications with fluctuating input voltage. The paper details the interaction of topology and the switching control process to achieve optimal performance. Experimental results are provided, comparing switching efficiency, energy loss, and stability under real-world solar system conditions, confirming the design's feasibility and offering recommendations for optimizing renewable energy applications.

2. Proposed single-phase current-fed inverter

The proposed topology for the single-phase four-switch current-fed common-ground inverter (4S-CFCGI) is depicted in Figure 1. It consists of 4 active switches represented by mosfets (S_1-S_4), 5 diodes with 2 diodes (D_0, D_1) in the midle of inverter part and 3 diodes (D_a, D_b, D_c) in the impedance network, 1 capacitor (C_1) and 2 inductors (L_1, L_2). Switched - Inductor imdepance network (SI)is placed in front to enhance DC-link voltage amplitude. By connected ground between the load terminal and the voltage input terminal, leakage current is actually eliminated. Three time intervals within a period are used to describe the operating principle. Four time periods in a cycle are divided to analyze the operating principle of the topology. With d_1 being the duty cycle when the configuration operates in positive or negative inverter state, d_2 and d_3 are duty cycles representing the operating period in zero state (when

JTE HCMUTE
ISSN: 2615-9740
JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Education
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

only switch S_4 is turned-on. The remaining d_4 represents the shoot-through state (ST-state) period when S_1, S_2 and S_3 are turned-on.

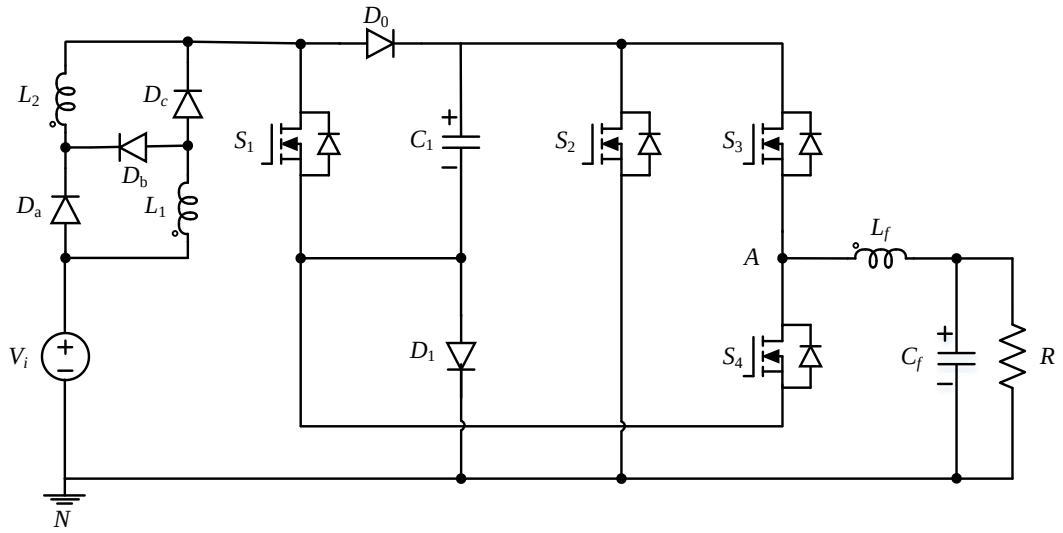

Figure 1. *Single-phase four-switch current-fed inverter topology.*

2.1. The operating concept of the 4S-CFCGI

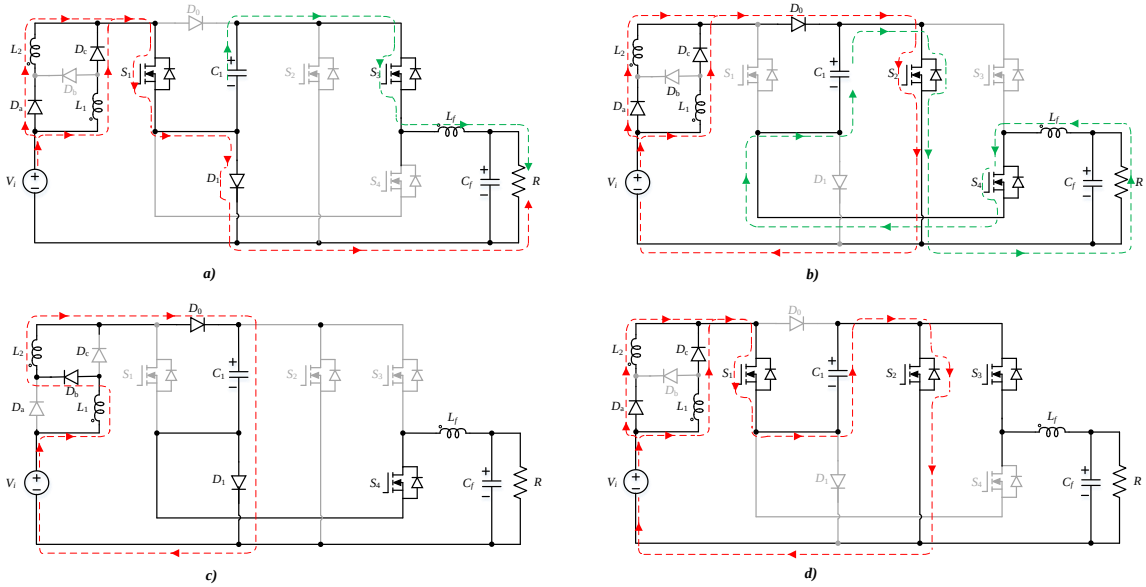

Figure 2. *Equivalent circuit in operating states:*
a) Positive state, b) Negative state, c) Zero state, d) Shoot-through state.

Figure 2(a) illustrates the operating principle of the 4S-CFCGI in its positive state. In this mode, switches S_1 and S_3 are turn-on, while switches S_2 and S_4 remain turn - off. During this time (d_1T_s), energy is stored in inductors L_1 and L_2. Diodes D_a and D_c are forward-biased, whereas diode D_b is reverse-biased. Additionally, when the input current surpasses the load current, diode D_1 becomes forward-biased. Based on the equivalent circuit, it can be observed that during the time intervals d_1T_s and $(1-d_1)T_s$, the voltage across the inductors (v_{L_1}, v_{L_2}) in the switched inductor (SI) network, the current through capacitor C_1 (i_{C1}), and the peak of output voltage ($\hat{v}_o$) can be analyzed:

$$v_{L1} = -v_{L2} = V_{in} \tag{1}$$

$$i_{C_1} = -i_o \tag{2}$$

$$\hat{v}_o = v_{C_1} \tag{3}$$

In contrast to the positive state, in the negative state, switches S_2 and S_4 turn - on, S_1 and S_3 turn-off. Diode D_0 is forward biased while D_1 is reverse biased as shown in Figure 2(b). The impedance network still operates similarly to the positive state. The voltage and current equations and the voltage across the inductor of SI, capacitor and output voltage are determined as follows:

$$v_{L1} = -v_{L2} = V_{in} \tag{4}$$

$$i_{C_1} = i_o \tag{5}$$

$$\hat{v}_o = -v_{C_1} \tag{6}$$

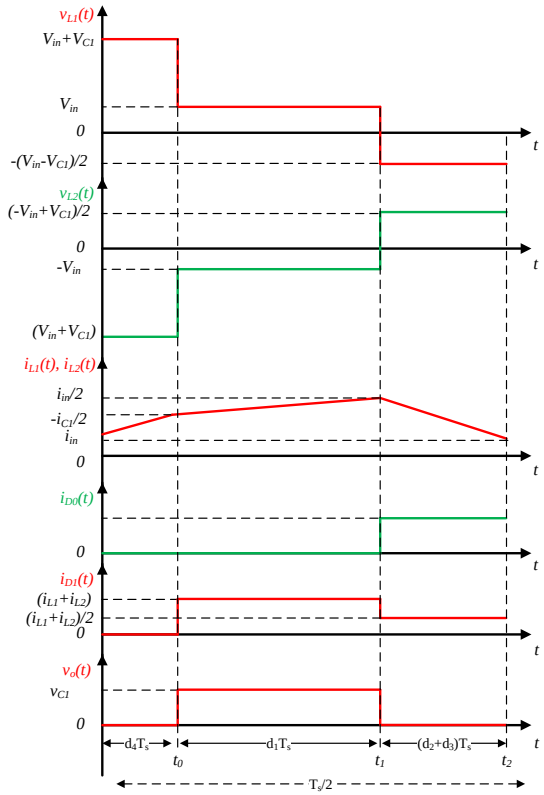

Figure 3. *Waveforms of current and voltage across the diode and inductor during a positive period.*

The proposed topology operates similarly in both positive and negative cycles when in normal mode, as can be observed from equations (1) through (6). However, they are symmetrical in comparison to the current waveform.

In the zero-state state in Figure 2(c), only switch S_4 turns-on. D_0 and D_1 are both forward biased. At this time, capacitor C_1 is charged by V_{in} and energy from inductors L_1, L_2. This time period is represented by $(d_2+d_3)T_s$, and the output voltage is 0. The voltage across the inductor in SI, and the current across the capacitor are as follows:

$$v_{L1} = -v_{L2} = \frac{V_{in} - V_{C_1}}{2} \tag{7}$$

$$i_{C_1} = i_{L_1} = i_{L_2} \tag{8}$$

In the shoot-through state in Figure 2(d), switches S_1, S_2, S_3 turn-on. D_0 and D_1 are forward biased, inductors L_1 and L_2 continue to charge when Da and Dc are forward biased. d_4T_s is represented for this period. Similar to above, the equationals are analyzed as follows:

$$v_{L1} = -v_{L2} = V_{in} + V_{C_1} \tag{9}$$

$$i_{C_1} = -(i_{L_1} + i_{L_2}) \tag{10}$$

Figure 3 shows the waveform and current on the inductor and diode of the SI network at the positive cycle.

2.2. Steady – state analysis.

When we use the inductor's voltage balancing method in steady state, we obtain the following equations:

$$V_{in}(1-d_1) + \left(\frac{V_{in} - V_{C_1}}{2}\right)(d_2 + d_3) + (V_{in} + V_{C1})d_4 = 0 \tag{11}$$

$$-i_o(1-d_1) + i_{L_1}(d_2 + d_3) - 2i_{L_1}d_4 = 0 \tag{12}$$

By observing the operating cycle in Figure 3, we can see that the operating time in positive inverter mode is equal to the sum of the remaining time periods in a cycle. From equations (11) and (12), we can determine the voltage across capacitor C_1 and the current of the inductor in steady state as follows:

$$V_{C1} = \hat{v}_o = \frac{V_{in}(1 - d_2/2 - d_4)}{\frac{d_2}{2} - d_4} \tag{13}$$

$$i_{L_1} = i_{L_2} = \frac{i_o(1 - d_2 - 2d_4)}{d_2} \tag{14}$$

From equations (13) and (14). We can calculate the boost factor B and the voltage gain G as follows:

$$B = \frac{V_{C1}}{V_{in}} = \frac{1 - d_2/2 - d_4}{\frac{d_2}{2} - d_4} \tag{15}$$

$$G = m.B = m.\frac{1 - d_2/2 - d_4}{\frac{d_2}{2} - d_4} \tag{16}$$

where m is the modulation index ($m \le 1$)

2.3. Leakage current analysis

The operation of the inverter involves switching between different states, which results in the generation of high-frequency common-mode voltage (CMV). In the proposed inverter topology, the coupling ground (CG) establishes a direct connection between the input and the output, which could either be an AC load or the utility grid. This configuration helps manage voltage fluctuations but also influences the overall voltage and current behavior of the system. In addition to CMV, the differential

mode voltage plays a significant role in affecting the circulating current within the inverter. This circulating current, combined with the CMV, can impact the efficiency and electromagnetic compatibility (EMC) of the system. To better understand these effects, the simplified expressions for the total common-mode voltage (CMV) and leakage current (i_{lkg}) are derived as foll

$$v_{CMV} = \frac{v_o}{2} \tag{17}$$

$$i_{lkg} = C_{PV} \frac{dv_{CMV}}{dt} \tag{18}$$

Where Cpv is represented by the parasitic capacitance component in the ground between the source and the load. Typically they have values of 10-12pF.

3. Pulse Width Modulation Scheme

The proposed inverter employs the unipolar Pulse Width Modulation (PWM) control technique to generate the switching pulses. This technique offers significant advantages, such as the effective elimination of center-band harmonics and a substantial reduction in the size and complexity of the output filter, improving overall system efficiency and performance. To generate the switching pulses, a high-frequency triangular carrier signal is used. This carrier signal is compared with two modulating reference signals, $v_{ref1}(t)$ and $v_{ref2}(t)$,which are phase-shifted by 180°. Additionally, the system incorporates two constant amplitude offset signals, V_{ST} and -V_{ST}. Figure 4 shows the turn-on and turn-off order of the switches in one switching cycle. Table 1 shows the on-off sequence of the switches and diode corresponding to the output voltage levels The reference voltage signal equation is described in formulas (19) and (20):

$$v_{ref1} = m\sin(\theta) \tag{19}$$

$$v_{ref2} = m.\sin\left(\theta + \frac{\pi}{2}\right) \tag{20}$$

$$V_{ST} = -V_{ST} = m \tag{21}$$

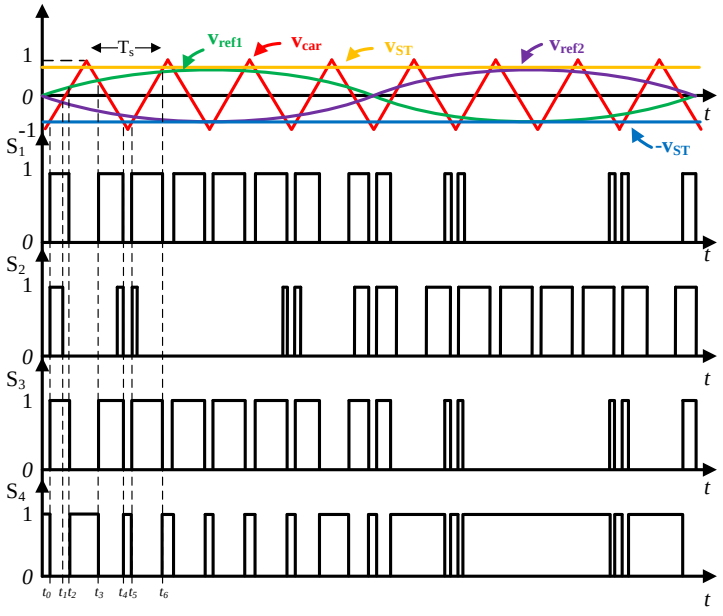

Figure 4. *Waveforms of gating signals of control technique for the 4S-CFCGI.*

JTE HCMUTE
ISSN: 2615-9740
JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Education
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

Table 1. *The switching states and the output voltage of 4S-CFCGI.*

Mode	State of Diode					State of Switches				Output voltage
	D_a	D_b	D_c	D_0	D_1	S_1	S_2	S_3	S_4	
Positive	ON	OFF	ON	OFF	ON	ON	OFF	ON	OFF	$+V_{C1}$
Negative	ON	OFF	ON	ON	OFF	OFF	ON	OFF	ON	$-V_{C1}$
Zero	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	ON	0
Shoot-through	ON	OFF	ON	OFF	OFF	ON	ON	ON	OFF	0

During the d_2T_S period, PWM pulses are generated by comparing the triangular carrier signal with the reference levels of $\pm V_{ST}$. These reference levels represent the upper and lower bounds of the modulation, ensuring that the carrier signal triggers the pulse whenever it crosses these thresholds. In contrast, during the d_4T_S period PWM signals are produced by monitoring the behavior of the triangular carrier signal relative to the modulating signal and a constant amplitude signal. Specifically, a pulse is developed when the triangular signal falls within the range defined by the modulating signal and the constant amplitude reference. This mechanism allows for more precise control and modulation, adapting the pulse characteristics to the desired signal profiles during this period. For the relationships between time periods included $d_1 = d_2 + d_3 + d_4$ and $d_3 = d_4$.

4. Ouput Low-pass LC filter

To suppress high-frequency switching noise and meet standards such as IEC (THD<5%), a second-order LC low-pass filter is commonly used at the inverter output. This filter attenuates harmonics above a chosen cutoff frequency (f_c) allowing lower-frequency components (primarily the fundamental to pass). A design parameters include the cutoff frequency and quality factor Q which respectively determine harmonic attenuation and frequency selectivity. While a lower f_c enhances THD performance, it may reduce system bandwidth. Similarly, a high Q improves selectivity but increases phase lag, impairing dynamic response. A typical design adopts $Q = 0.707$ (Butterworth response) for optimal trade-off between flatness and damping. To ensure effective filtering without affecting the output power, f_c s often set to one-tenth of the switching frequency, with corresponding L_f and C_f values derived according:

$$f_c = \frac{1}{10} f_s = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{22}$$

$$Q = R\sqrt{\frac{C_f}{L_f}} \tag{23}$$

From (22) and (23), we have:

$$\begin{cases} L_f C_f = \dfrac{25}{\pi^2 f_s^2} \\ \dfrac{C_f}{L_f} = \dfrac{Q^2 P_o^2}{V_{o\_rms}^4} \end{cases} \tag{24}$$

So that:

$$\begin{cases} L_f \geq \dfrac{5V_{o\_RMS}^2}{\pi f_s Q P_o} \\ C_f \geq \dfrac{5QP}{\pi f_s V_{o\_RMS}^2} \end{cases} \quad (25)$$

5. Results Analysis

Table 2. *Parameters used in simulation.*

Parameter/Components		Unit
Input voltage	V_{in}	10.5 V
Output voltage (Point to Ground)	V_o	220 V_{RMS}
Inductor	L_1, L_2	*500µH*
Capacitor	C_1	*680µF/400V*
Carrier frequency	f_s	10 kHz
LC fillter	L_f and C_f	5 mH and 10 µF
Modulation index	m	0.8
Load	R	12 Ω

To evaluate the performance of the 4S-CFCGI, comprehensive simulation studies of the inverters were conducted using PSIM. The circuit parameters utilized in the simulations are detailed in Table 2.

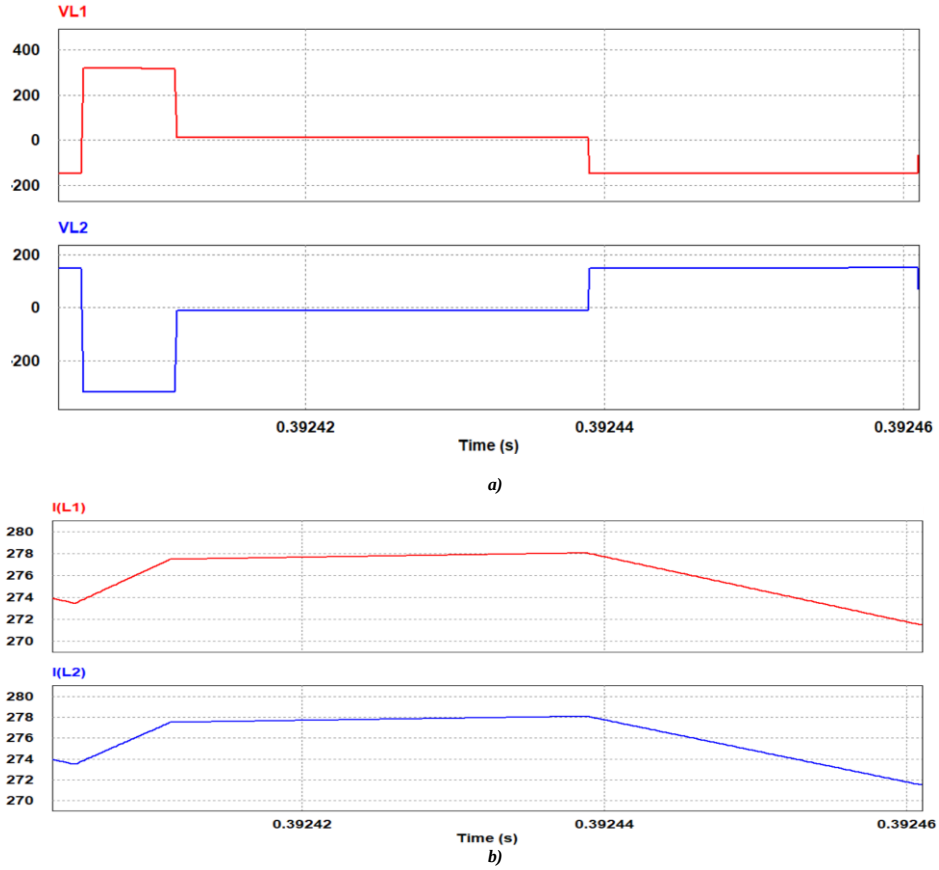

Figure 5. *a) Voltage profile results on inductors L_1 and L_2, b) Current profile results on inductors L_1 and L_2.*

Figure 5(a) shows the voltage waveform profiles across inductors L_1 and L_2 during one switching period . It can be seen that the voltage waveforms of the two inductors are symmetrical. The voltage simulation results show the changes at different time intervals, such as at time interval inverter (positive) is $V_{L1} = -V_{L2} = V_{in} = 10.5\,V_{dc}$, at time interval zero-state is $V_{L1} = -V_{L2} = \dfrac{V_{in} - V_{C_1}}{2} = 275\,V_{dc}$ and time interval shoot-through mode is $V_{L1} = -V_{L2} = V_{in} + V_{C_1} = 318\,V_{dc}$. Similarly, the current values across the inductors in the SI network also correspond to the theoretical analysis at the time interval.

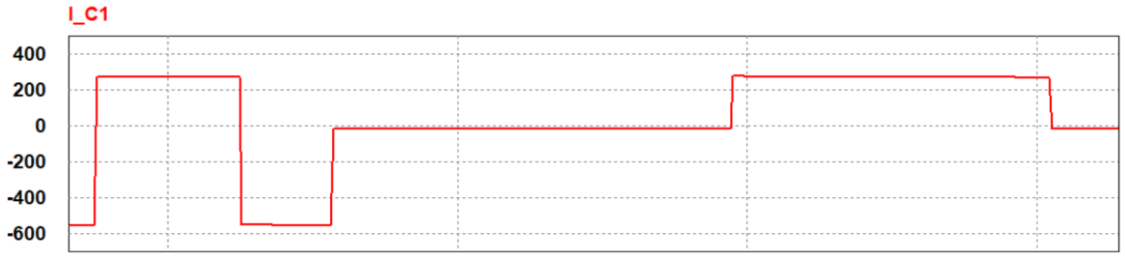

Figure 6. *Current waveform on capacitor C_1.*

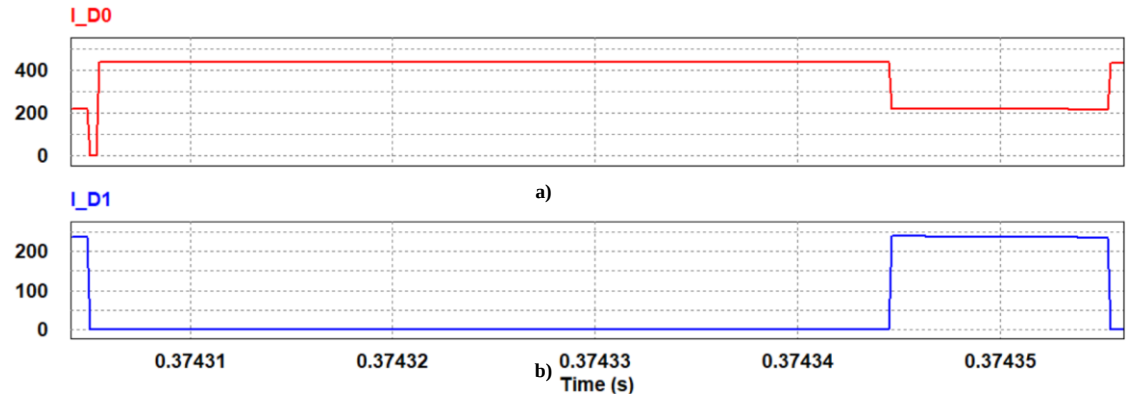

Figure 7. *a) Current through diode D_0, b) Current through diode D_1.*

The current waveform of capacitor C1 is shown in Figure 6. At time d1 (positive or negative) $i_{C1} = i_o = -12.6\,A$, at time d2+d3 $i_{C1} = i_{L_1} = i_{L_2} = 275\,A$. And at time d4 $i_{C_1} = -(i_{L_1} + i_{L_2}) = -551\,A$. Figure 7 shows the current through diode D_1 and diode D_2.

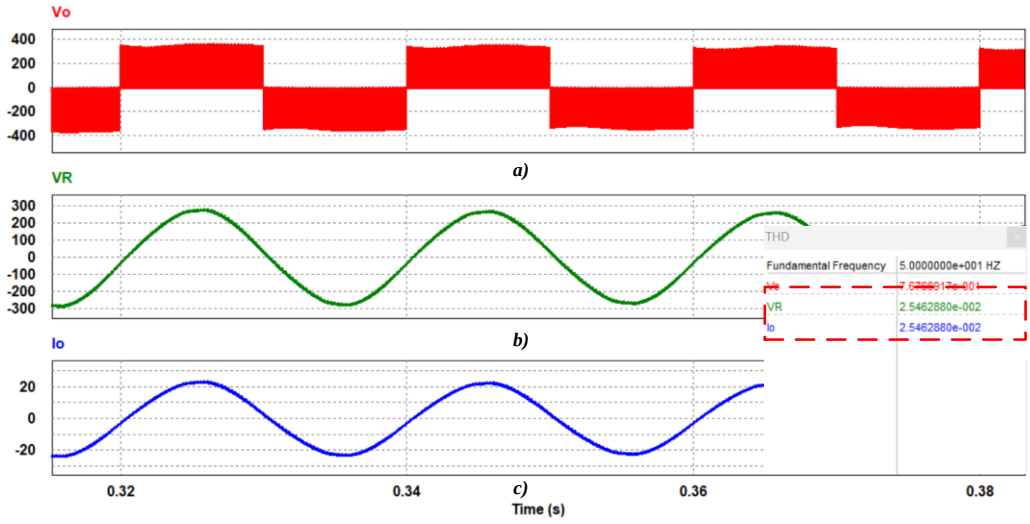

Figure 8. *a) Ouput voltage waveform (Point A to Ground), b) Ouput voltage waveform on Load, c) Ouput current waveform.*

Figure 8(a) shows the output voltage waveform, with three voltage levels as analyzed, the result reaches the value of $220V_{RMS}$. Figure 8(b) and 8(c) shows the ouput voltage waveform *on load* and the output current waveform. With the filter parameters specified as L_f = 5 mH and C_f = 10 µF, the resulting THDu and THDi are approximately 2.5% at fundamental frequency of 50Hz.

Based on the output voltage simulation results in Figure 8(a), we can see that the output voltage waveform has only 3 main levels: Positive, zero and Negative. Based on the analysis as in [9], we can conclude that $V_{CMV} = \frac{V_o}{2}$ and is a constant throughout the cycle. Therefore, $\frac{dV_{CMV}}{dt} = 0$ so i_{lkg} in equation (18) is zero, thereby eliminating the leakage current.

Table 3. *Comparison Study.*

	Ref.[10]	Ref.[13]	Ref.[15]	Ref.[17]	Proposed
Device count (*L*/C/S/D)	0/0/6/2	2/4/4/3	1/1/5/1	1/1/5/1	2/1/4/5
Input current	Disc.	Cont.	Disc.	Cont.	Cont.
Maximum Voltage Stress on Switch	V_o	$2V_o$	V_o	V_o	V_o
Boost Factor	*N/A*	*N/A*	$\frac{1-d_2}{d_2}$	$\frac{1}{d_2}$	$\frac{1-d_2/2-d_4}{\frac{d_2}{2}+d_4}$
Gate driver	*4*	*4*	3	3	3
Leakage Current	*45 mA*	≈ 0	≈ 0	≈ 0	≈ 0

L: Inductor, C: Capacitor, S: Switch, D0: Diode, Disc.: Discontinuous, Cont.: Continuous, N/A: Not Applicable

To show the improvement of the proposed 4S-CFCGI topology with the conventional topology, a comparison is shown in Table 3. The detailed comparison is given in terms of the number of components, input current, voltage stress, boost factor, number of gate driver and leakage current. In terms of the number of components, in 4S-CFCGI there may be more passive components than some traditional structures, however the design size can be small so the performance, size and weight are all better.

6. Conclusions

This paper examines the 4S-CFCGI inverter, a novel design that incorporates only four active switches, a SI network, and a capacitor. The proposed inverter effectively addresses the issue of leakage current while achieving enhanced voltage gain, which enables reliable and efficient operation. The findings demonstrate that the inverter delivers a continuous input current, a critical advantage for photovoltaic (PV) systems. Moreover, the symmetrical operation of the inverter, combined with the use of a single DC capacitor during both half-cycles, prevents the injection of DC offset current into the grid. To underscore the benefits of the proposed design, a detailed comparison of its features with those of recently developed grid-tied inverters is presented, highlighting its superior performance and operational advantages.

Acknowledgments

This work belongs to the project grant number T2025-220 funded by Ho Chi Minh City University of Technology and Education, Vietnam.

Conflict of Interest

The authors declare no conflict of interest.

REFERENCES

[1] R. M. Elavarasan *et al.*, "A Comprehensive Review on Renewable Energy Development, Challenges, and Policies of Leading Indian States With an International Perspective," in *IEEE Access*, vol. 8, pp. 74432-74457, 2020.
[2] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of Traditional Inverters and Z -Source Inverter for Fuel Cell Vehicles," in *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1453-1463, July 2007.
[3] I. Jamal, M. F. Elmorshedy, S. M. Dabour, E. M. Rashad, W. Xu, and D. J. Almakhles, "A Comprehensive Review of Grid-Connected PV Systems Based on Impedance Source Inverter," in *IEEE Access*, vol. 10, pp. 89101-89123, 2022.
[4] F. Z. Peng, "Z-source inverter," in *IEEE Transactions on Industry Applications*, vol. 39, no. 2, pp. 504-510, March-April 2003.
[5] J. Anderson and F. Z. Peng, "Four quasi-Z-Source inverters," *2008 IEEE Power Electronics Specialists Conference*, Rhodes, Greece, 2008, pp. 2743-2749.
[6] A. Ravindranath, S. K. Mishra, and A. Joshi, "Analysis and PWM Control of Switched Boost Inverter," in *IEEE Transactions on Industrial Electronics*, vol. 60, no. 12, pp. 5593-5602, Dec. 2013.
[7] S. S. Nag and S. Mishra, "Current-Fed Switched Inverter," in *IEEE Transactions on Industrial Electronics*, vol. 61, no. 9, pp. 4680-4690, Sept. 2014.
[8] M. K. Nguyen and T. T. Tran, "A Single-Phase Single-Stage Switched-Boost Inverter With Four Switches," in *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6769-6781, Aug. 2018.
[9] T. K. S. Freddy, N. A. Rahim, W. P. Hew, and H. S. Che, "Comparison and Analysis of Single-Phase Transformerless Grid-Connected PV Inverters," in *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5358-5369, Oct. 2014.
[10] B. Ji, J. Wang, and J. Zhao, "High-Efficiency Single-Phase Transformerless PV H6 Inverter With Hybrid Modulation Method," in *IEEE Transactions on Industrial Electronics*, vol. 60, no. 5, pp. 2104-2115, May 2013
[11] S. Jahan, M. F. Kibria, S. P. Biswas, M. R. Islam, M. A. Rahman, and K. M. Muttaqi, "H9 and H10 Transformer-Less Solar Photovoltaic Inverters for Leakage Current Suppression and Harmonic Current Reduction," in *IEEE Transactions on Industry Applications*, vol. 59, no. 2, pp. 2446-2457, March-April 2023
[12] Y. P. Siwakoti and F. Blaabjerg, "Common-Ground-Type Transformerless Inverters for Single-Phase Solar Photovoltaic Systems," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 3, pp. 2100-2111, March 2018
[13] F. Peng, G. Zhou, N. Xu, and S. Gao, "Zero Leakage Current Single-Phase Quasi-Single-Stage Transformerless PV Inverter with Unipolar SPWM," in *IEEE Transactions on Power Electronics*, vol. 37, no. 11, pp. 13755-13766, Nov. 2022
[14] D. V. Bui and H. Cha, "Split-Phase Boost PWM AC-AC Converter with Inherent Output Voltage Balancing," *2021 24th International Conference on Electrical Machines and Systems (ICEMS)*, Gyeongju, Korea, Republic of, 2021, pp. 208-212
[15] P. K. Chamarthi, M. S. E. Moursi, V. Khadkikar, K. H. A. Hosani, A. Al-Durra, and T. H. M. EL-Fouly, "A Single Stage Doubly Grounded Transformerless Inverter Topology With Buck-Boost Voltage Capability for Grid Connected PV Systems," in *IEEE Transactions on Power Delivery*, vol. 37, no. 6, pp. 5044-5058, Dec. 2022
[16] D. T. Do, V. T. Tran, T. D. B. Thi, N. H. V. Thi, and M. K. Nguyen, "A Single-Phase Buck-Boost Derived Common-Ground Inverter," *2023 11th International Conference on Power Electronics and ECCE Asia (ICPE 2023 - ECCE Asia)*, Jeju Island, Korea, Republic of, 2023, pp. 1873-1877
[17] H. Tian, M. Chen, G. Liang, and X. Xiao, "A Single-Phase Transformerless Common-Ground Type PV Inverter with Active Power Decoupling," in *IEEE Transactions on Industrial Electronics*, vol. 70, no. 4, pp. 3762-3772, April 2023
[18] R. Ravitheja, M. Sahoo, P. Shaw, and K. Thirumala, "A Four Switch Common Ground-Based Single Phase Current-Fed Boost Inverter," in *IEEE Transactions on Power Electronics*, vol. 40, no. 1, pp. 1064-1073, Jan. 2025.

Duc Tri Do was born in Vietnam in 1973. He received the B.S., M.S. and Ph.D degrees in electronic engineering from the Ho Chi Minh City University of Technology and Education, Ho Chi Minh City, Vietnam, in 1999, 2012 and 2021, respectively. He is currently a Lecturer with the Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology and Education. His current research interests include power converters for renewable energy systems.
Email: tridd@hcmute.edu.vn. ORCID: https://orcid.org/0000-0002-4096-5208

Bich Nga Truong Thi received the B.S. degree in electronic and eletrical engineering from Ho Chi Minh City University of Technology and Education (HCMUTE) , Vietnam, in 1997 and the M.S. degree in electronics and telecommunications from Ho Chi Minh City University of Technology (HCMUT), Vietnam, in 2003. She has been a lecturer of the Faculty of Electronic and Electrical Engineering at HCMUTE, Viet nam. Her research interests include the electronic circuits and FPGA.
Email: tridd@hcmute.edu.vn. ORCID: https://orcid.org/0000-0001-7735-1552

Tan Hung Nguyen received the B.S degree in Electrical and Electronic engineering and the M.S. degree in electrical engineering from the Ho Chi Minh City University of Technology and Education, Ho Chi Minh City, Vietnam, in 2022 and 2024, respectively. His current research interests include the topologies and control of dc-dc converters and dc-ac inverters.
Email: hungnt169@fe.edu.vn. ORCID: https://orcid.org/0009-0005-1793-1383