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# High Step-Up DC-DC Converter Using Switching Cells for PV Applications

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**ABSTRACT**

In the context of a rapidly evolving global energy landscape transitioning towards renewable energy sources, the need for innovative, efficient, and flexible power conversion technologies has become increasingly critical. This paper presents a high step-up DC-DC converter using switching cells with a single switch for photovoltaic (PV) applications. The proposed topology features a simplified structure with only one switch, combining switched cells with inductors and capacitors. This feature helps to reduce the current stress through the inductor and the voltage stress on the capacitor. This design achieves high step-up conversion with a small duty cycle while maintaining simplicity in control and low voltage stress on the semiconductor devices. These attributes contribute to an overall improvement in the converter's efficiency. The paper provides a comprehensive analysis in continuous conduction mode (CCM) and details the design of components, emphasizing the practicality and feasibility of the proposed topology. The operation of the proposed converter is validated through comprehensive 200-W/20-kHz simulation results, carried out using PSIM software.

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## 1. Introduction

In recent times, renewable energy sources have gained significant attention as a sustainable solution for the future, particularly as traditional fossil fuel reserves continue to deplete. Additionally, the urgent challenges posed by climate change and global warming, largely driven by rising greenhouse gas emissions, have emphasized the need for cleaner energy alternatives. Among various renewable options, photovoltaic (PV) solar energy has emerged as a key focus, with rapid advancements in PV panel technology and deployment. However, PV arrays typically generate low and unstable voltage outputs [1], necessitating the use of high boost converters to elevate their voltage levels and align them with power grid requirements [2], [3]. An illustration of the distributed generation systems for PV arrays is provided in Figure 1. To bridge the gap between PV solar energy and high-voltage DC bus systems, step-up DC-DC converters play a crucial role by ensuring efficient power conversion [4]. Besides providing high voltage gain, DC-DC converters used in PV systems must also fulfill several important criteria: 1) Low ripple on input current; 2) Low voltage stress on components; 3) Maintaining a common ground between the input and output help prevent common-mode leakage current, thereby reducing electromagnetic interference and enhancing system reliability [5].

When considering isolation in DC-DC converters, they can be divided into two main categories: isolated and non-isolated. Isolated DC-DC converters incorporate high-frequency transformers to create electrical separation between the input and output. While this approach ensures isolation, it often results in increased size and cost. Additionally, designing high-frequency transformers poses challenges, with their size becoming a major drawback. Furthermore, active switches in such systems often experience high voltage stress due to leakage inductance in transformers [6]. Many coupled-inductor topologies have been proposed [7]; however, the design of these topologies remains challenging. Consequently, non-isolated configurations offer a practical alternative, delivering high voltage conversion with enhanced efficiency and cost-effectiveness, particularly in sustainable energy applications [8].

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The basic boost converter is widely used due to its simplicity and cost-efficiency. However, this type of converter requires a sufficiently large duty cycle to meet the voltage conversion demands of practical applications. Such operation results in significant power losses in the switching components and boost inductors [9]. To overcome these drawbacks, recent years have seen the development of innovative structures aimed at improving the high-voltage conversion capabilities of DC-DC converters. In [10], a single switch transformerless topology with an $L^2C^3D^2$ network and common ground for fuel cell vehicles was mentioned, but its gain is still limited. Meanwhile, in [11], a non-isolated with quadratic structure was introduced with high gain, but it still imposes significant stress on components, leading to reduced efficiency and reliability. The non-isolated topology referenced in [12] features a single switch and a switched-inductor. This structure can be extended by adding N cells to achieve higher gain in the converter.

Among these, switched-cell architectures incorporating inductors [13] and capacitors [14] have shown considerable potential, offering high power gain, scalability, and efficiency. These systems achieve voltage enhancement by leveraging the charging and discharging of energy stored in capacitors and inductors, arranged in parallel or series configurations. Furthermore, there has been growing interest in recently proposed hybrid structures that combine both switched-capacitor and switched-inductor cells [15]–[18]. This structure can provide high gain with a small duty cycle, which helps reduce stress on the components. The switched-inductor structure, where two inductors are connected in parallel on the input side, helps share the input current between both inductors, making the component design easier and increase the gain. Meanwhile, the switched-capacitor on the output side can double the gain of the converter while maintaining low voltage stress on the components. Additionally, both sides have the potential to be extended by adding N cells to achieve higher gain, with the stress distributed across all components. The structure proposed in this paper combines switched cells with inductors and capacitors and utilizes a single switch, making it easy to control and design.

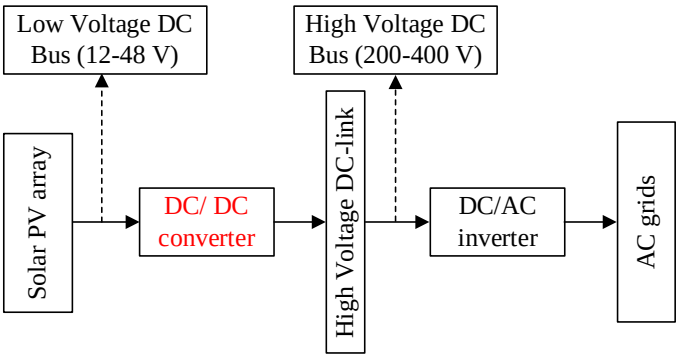


**Figure 1.** *Block diagram of High step-up DC-DC converter in PV application.*

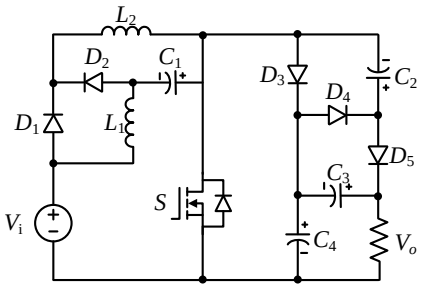


**Figure 2.** *Circuit diagram of proposed topology.*

This paper presents a high step-up DC-DC converter using switching cells for PV applications. The structure of the paper is organized as follows: Section 2 discusses the proposed converter and its operating analysis in continuous conduction mode. Section 3 outlines the design guidelines, while Section 4 presents the simulation results for verification. Section 5 compares the proposed converter with other high step-up DC-DC converters. Finally, Section 6 concludes the study with a summary of the key findings.

## 2. Structure and operating principle

### *2.1. Circuit structure*

The circuit structure of the proposed converter is shown in Figure 2. This structure of a single switch includes a switch *S*, five diodes $D_1$-$D_5$, four capacitors $C_1$-$C_4$, and two inductors $L_1$ and $L_2$.

### *2.2. Basic operating principle in CCM*

The following assumptions are considered in analyzing the steady-state operating principle:

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(1) All components are treated as ideal, neglecting forward voltage drops, on-state resistances of switches, and parasitic parameters.

(2) All inductors are assumed to have sufficiently high inductance to ensure operation in CCM, while the capacitors are considered to have adequate capacitance to maintain a stable voltage.

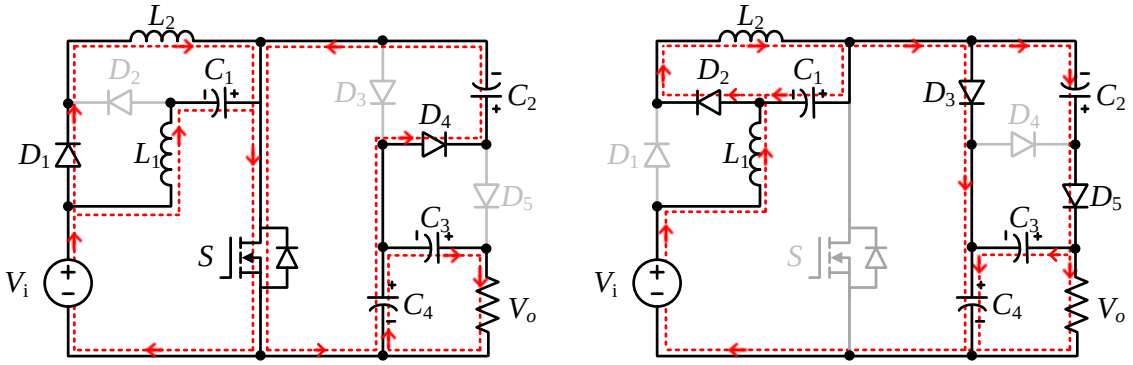


**Figure 3.** *Operating modes of the proposed converter: (a) Mode 1; (b) Mode 2.*

Mode 1 (0-*DT*): In this mode, the primary switch determines its operating state. During operation, diodes $D_1$ and $D_4$ are turned on while diodes $D_2$, $D_3$, and $D_5$ are turned off. Both inductors $L_1$ and $L_2$ are charged with energy by the input voltage $V_i$ through diode $D_1$ and switch $S$. Capacitors $C_2$, $C_1$ and load $R_o$ are charged by capacitors $C_3$ and $C_4$. The analysis circuit of the proposed converter is described in Figure 3(a). Using KVL, the corresponding equations are expressed as follows:

$$\begin{cases} v_{L1(ON)} = V_i + V_{C1} \\ v_{L2(ON)} = V_i \\ V_{C2} = V_{C4} \\ V_{C3} + V_{C4} = V_o, \end{cases} \tag{1}$$

Using KCL in this mode, the equation of the proposed converter can be obtained as:

$$\begin{cases} i_{L1} = -i_{C1(ON)} \\ i_{C3(ON)} = -I_o \\ i_{C4(ON)} = i_{C3(ON)} - i_{C2(ON)}, \end{cases} \tag{2}$$

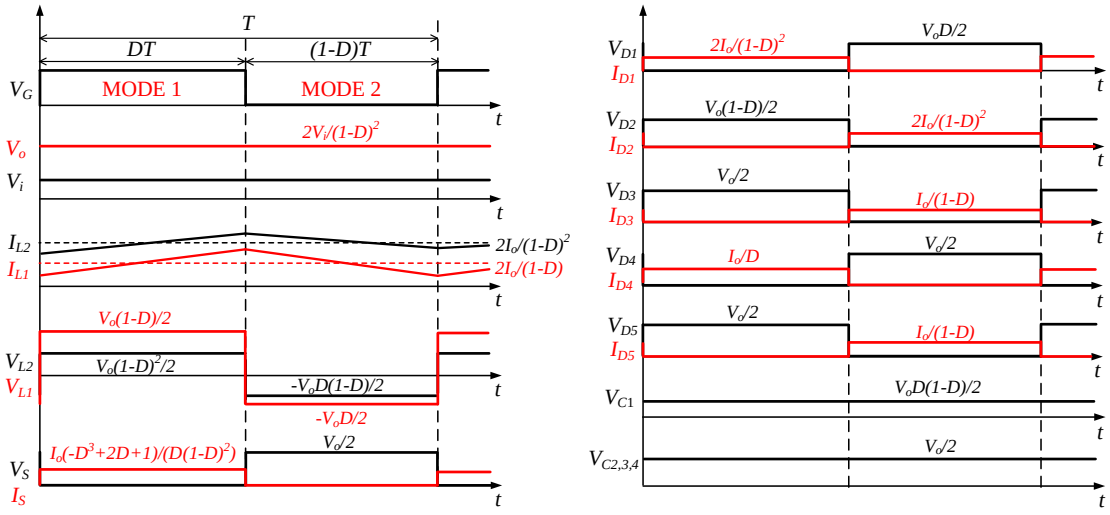


**Figure 4.** *Main waveforms of the proposed converter for CCM.*

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Mode 2 (*DT-T*): In this mode, switch *S* is turned off. In this operation mode, two diodes $D_1$ and $D_4$ are turned off, while three diodes $D_2$, $D_3$, and $D_5$ are turned on. Inductors $L_1$ and $L_2$, capacitors $C_1$ and $C_2$ discharge energy to the load and capacitors $C_3$ and $C_4$, respectively. The circuit analysis of the proposed converter is illustrated in Figure 3(b). Using the KVL, the relevant equations are expressed as follows:

$$\begin{cases} v_{L1(OFF)} = V_i + V_{C1} - V_{C4} \\ v_{L2(OFF)} = -V_{C1} \\ V_{C2} = V_{C3}, \end{cases} \tag{3}$$

Using the KCL, the equations are shown below:

$$\begin{cases} -i_{C2(OFF)} = i_{C3(OFF)} + I_o \\ i_{L1} + i_{C1(OFF)} = i_{L2} \\ i_{L2} + i_{C3(OFF)} + i_{C2(OFF)} = i_{C1(OFF)} + i_{C4(OFF)}, \end{cases} \tag{4}$$

Using the average value equation of the inductor voltage:

$$\langle v_{L1} \rangle_T = \langle v_{L2} \rangle_T = 0, \tag{5}$$

From equations (1), (3), and (5) the voltage stress on capacitor and inductor of the proposed converter can be dervied:

$$\begin{cases} V_{C1} = \dfrac{DV_i}{1-D} \\ V_{C2} = V_{C3} = V_{C4} = \dfrac{V_i}{(1-D)^2}, \end{cases} \tag{6}$$

$$\begin{cases} V_{L1(ON)} = \dfrac{(1-D)}{2} V_o \\ V_{L2(ON)} = \dfrac{(1-D)^2}{2} V_o \end{cases} \& \begin{cases} V_{L1(OFF)} = -\dfrac{D}{2} V_o \\ V_{L2(OFF)} = -\dfrac{D(1-D)}{2} V_o, \end{cases} \tag{7}$$

The voltage gain of the proposed converter is determined as follow:

$$G = \frac{V_o}{V_i} = \frac{2}{(1-D)^2}, \tag{8}$$

The balance related to the capacitor principle can be applied to capacitors $C_1$, $C_2$, $C_3$, and $C_4$ as follows:

$$\langle i_{C1,2,3,4} \rangle_T = 0, \tag{9}$$

From (2), (4), and (9), the capacitors $C_1$, $C_2$, $C_3$, and $C_4$ currents in each operation mode can be calculated as follows:

$$\begin{cases} I_{C1(ON)} = \dfrac{-2}{1-D} I_o \\ I_{C2(ON)} = \dfrac{1}{D} I_o \\ I_{C3(ON)} = -I_o \\ I_{C4(ON)} = -\dfrac{1+D}{D} I_o \end{cases} \& \begin{cases} I_{C1(OFF)} = \dfrac{2D}{(1-D)^2} I_o \\ I_{C2(OFF)} = \dfrac{-1}{1-D} I_o \\ I_{C3(OFF)} = \dfrac{D}{1-D} I_o \\ I_{C4(OFF)} = \dfrac{1+D}{1-D} I_o, \end{cases} \tag{10}$$

Based on the current through capacitor in each mode and Figure 3, the RMS current of capacitor is given as:

$$\begin{cases} I_{C1,RMS} = 2I_o\sqrt{\dfrac{D}{(1-D)^3}} \\ I_{C2,RMS} = I_o\sqrt{\dfrac{1}{D(1-D)}} \end{cases} \& \begin{cases} I_{C3,RMS} = I_o\sqrt{\dfrac{1}{1-D}} \\ I_{C4,RMS} = I_o\dfrac{1+D}{\sqrt{D(1-D)}}, \end{cases} \tag{11}$$

From the capacitor current in each mode, the inductor current and input current are derived as:

$$\begin{cases} I_{L1} = \dfrac{2}{1-D}I_o \\ I_{L2} = \dfrac{2}{(1-D)^2}I_o \\ I_i = \dfrac{2}{(1-D)^2}I_o, \end{cases} \tag{12}$$

## 3. Design guideline

### *3.1. Inductor design*

The inductance is chosen based on the current ripple through it. From Figure 4, we have:

$$\begin{cases} v_{L1} = L_1\dfrac{di_{L1}}{dt} \\ v_{L2} = L_2\dfrac{di_{L2}}{dt} \end{cases} \Leftrightarrow \begin{cases} v_{L1} = L_1\dfrac{\Delta I_{L1}}{\Delta t} \\ v_{L2} = L_2\dfrac{\Delta I_{L2}}{\Delta t}, \end{cases} \tag{13}$$

From equations (12) and (13), the inductance values of $L_1$ and $L_2$ can be calculated as:

$$\begin{cases} L_1 = \dfrac{D(1-D)}{2\Delta I_{L1}f}V_o \\ L_2 = \dfrac{D(1-D)^2}{2\Delta I_{L2}f}V_o, \end{cases} \tag{14}$$

Where: $\Delta I_L$ is the current ripple of inductor.

### *3.2. Capacitor design*

The capacitance is selected in consideration of the current ripple passing through it. Referring to Figure 4, equations (10) and (15), we observe:

$$\begin{cases} i_{C1} = C_1\dfrac{\Delta v_{C1}}{\Delta t} \\ i_{C2} = C_2\dfrac{\Delta v_{C2}}{\Delta t} \\ i_{C3} = C_3\dfrac{\Delta v_{C3}}{\Delta t} \\ i_{C4} = C_4\dfrac{\Delta v_{C4}}{\Delta t} \end{cases} \Leftrightarrow \begin{cases} C_1 = \dfrac{2D}{(1-D)\Delta v_{C1}f}I_o \\ C_2 = \dfrac{1}{\Delta v_{C2}f}I_o \\ C_3 = \dfrac{D}{\Delta v_{C3}f}I_o \\ C_4 = \dfrac{1+D}{\Delta v_{C4}f}I_o, \end{cases} \tag{15}$$

Where: $\Delta V_C$ is the voltage ripple on capacitor.

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### *3.3. Semiconductor design*

In general, the design of semiconductor devices, such as single switch and power diodes, adheres to specific voltage and current ratings, which should surpass the theoretical calculations. The voltage and current stresses on the switch and diodes in the proposed converter are determined through equations (6)-(8), (10), (12) and Figure 3, respectively:

$$\begin{cases} V_S = \dfrac{V_i}{(1-D)^2}, \\ V_{D1} = \dfrac{DV_i}{(1-D)^2}, \\ V_{D2} = \dfrac{V_i}{1-D}, \\ V_{D3} = V_{D4} = V_{D5} = \dfrac{V_i}{(1-D)^2} \end{cases} \& \begin{cases} I_S = \dfrac{(-D^2+2D+1)I_o}{D(1-D)^2} \\ I_{D1} = I_{D2} = \dfrac{2I_o}{(1-D)^2} \\ I_{D3} = I_{D5} = \dfrac{I_o}{1-D} \\ I_{D4} = \dfrac{I_o}{D}, \end{cases} \tag{16}$$

The RMS current through semiconductors can be derived from equation (17) and Figure 3:

$$\begin{cases} I_{S,RMS} = \dfrac{(-D^2+2D+1)I_o}{\sqrt{D}(1-D)^2} \\ I_{D1,RMS} = \dfrac{2\sqrt{D}I_o}{(1-D)^2} \\ I_{D2,RMS} = \dfrac{2I_o}{(1-D)^{3/2}} \end{cases} \& \begin{cases} I_{D3,RMS} = I_{D5,RMS} = \dfrac{I_o}{\sqrt{1-D}} \\ I_{D4,RMS} = \dfrac{I_o}{\sqrt{D}} \end{cases} \tag{17}$$

## 4. Simulation results

To validate the proposed converter, simulations are conducted to confirm the theory. The parameters of the proposed converter are listed in Table 1. According to the calculation in Section 3, two inductors with 0.5 mH are selected, all capacitors are used at 220 µF and the semiconductor devices are switching at 20 kHz. Figure 5 shows the simulation results for various parameters of the proposed converter, including input voltage, output voltage, voltage and current of inductor $L_1$, $L_2$, diode $D_1$ – $D_5$, switch $S$ and capacitor $C_1$-$C_4$. In this simulation, the input voltage is set at 25 V, achieving an output voltage of approximately 200 V and a power rating of 200 W, with a duty set to 50% of the cycle.

**Table 1.** *Parameters used for simulation.*

| Parameters | **Symbol** | **Value** |
|---|---|---|
| Input voltage | *Vi* | 25 V |
| Output voltage | *Vo* | 200 V |
| Power rating | *P* | 200 W |
| Switching frequency | *f* | 20 kHz |
| Inductor | $L_1$, $L_2$ | 0.5 mH |
| Capacitor | $C_1$, $C_2$, $C_3$, $C_4$ | 220 µF |

From Figure 5(a), the voltage stress on capacitor $C_1$ is approximately 25 V, while the voltage on capacitors $C_2$, $C_3$, and $C_4$ is half of the output voltage, around 100 V. In addition, in Figure 5(b), inductor $L_1$ has a measured current of 4.17 A with a peak-to-peak ripple of 2.34 A, and its RMS current is 4.23 A. Similarly, inductor $L_2$ has a measured current of 8.65 A, equal to its RMS current, with a peak-to-peak ripple of 1.14 A. In Figure 5(c), the average current stress on diodes $D_1$ and $D_2$ is 8 A, with an RMS current of 6.1 A, while for $D_3$, $D_4$, and $D_5$, the average current stress is 2.07 A, and the RMS currents are 1.58 A, 2.46 A, and 1.83 A, respectively. The current stress on switch S is 13.7 A, with an RMS current of 10.77 A. The voltage stresses on diodes $D_1$ and $D_2$ are 50 V, while the voltage stresses

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on the single switch and diodes D3, D4, and D5 are reverse-biased at half of the output voltage, approximately 100 V, as shown in Figure 5(d).

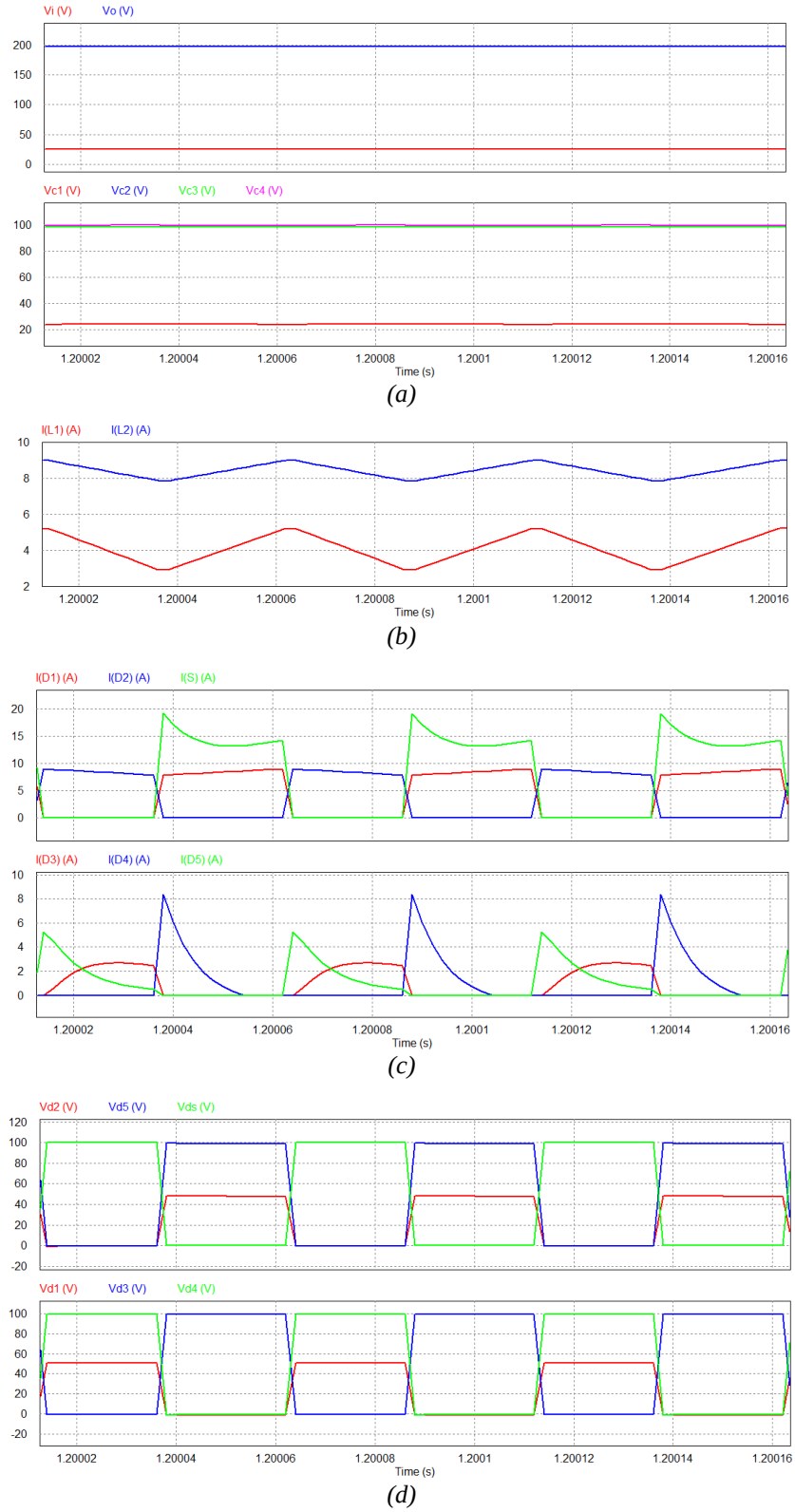


**Figure 5.** *Simulation of the proposed converter waveforms (a) Input voltage, output voltage and voltage stress on capacitors $C_1 – C_4$; (b) Current stress on inductors $L_1$ and $L_2$; (c) Current stress on diodes $D_1 – D_5$; (d) Voltage stress on diodes $D_1 – D_5$.*

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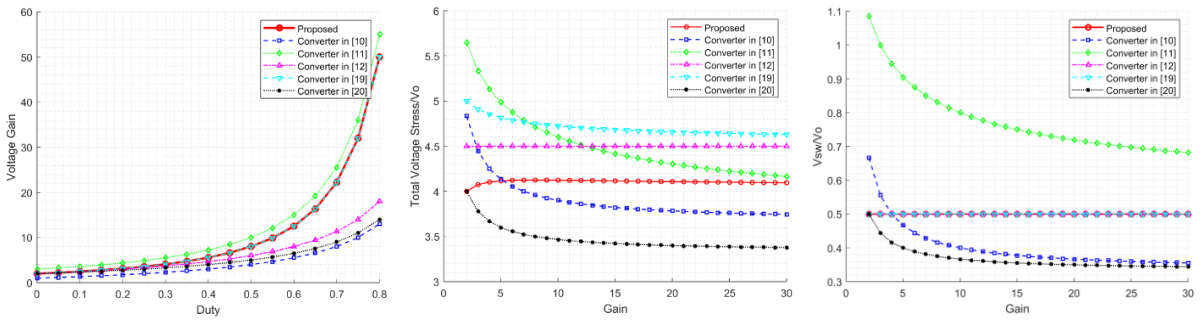
## 5. Comparison between the proposed converter and other structures

**Table 2.** *Comparative analysis of the proposed converter and other common high step-up DC-DC converters.*

| Converter | [10] | [11] | [12] | [19] | [20] | Proposed converter |
|---|---|---|---|---|---|---|
| Voltage gain | $\frac{1+2D}{1-D}$ | $\frac{3-D}{(1-D)^2}$ | $\frac{2(1+D)}{1-D}$ | $\frac{2}{(1-D)^2}$ | $\frac{2+D}{1-D}$ | $\frac{2}{(1-D)^2}$ |
| No. of Inductors | 3 | 2 | 2 | 2 | 2 | 2 |
| No. of Capacitors | 5 | 4 | 3 | 4 | 5 | 4 |
| No. of Diodes | 3 | 4 | 6 | 5 | 4 | 5 |
| No. of Switches | 1 | 2 | 1 | 1 | 1 | 1 |
| Total no. of Components | 12 | 12 | 12 | 12 | 12 | 12 |
| Voltage stress on Switch ($V_S/V_o$) | $\frac{1}{1+2D}$ | $\frac{3-2D}{3-D}$ | $\frac{1}{2}$ | $\frac{1}{2}$ | $\frac{1}{2+D}$ | $\frac{1}{2}$ |
| Total voltage stress ($V/V_o$) | $\frac{5+5D}{1+2D}$ | $\frac{16-9D}{3-D}$ | $\frac{9}{2}$ | $\frac{10-D}{2}$ | $\frac{8+2D}{2+D}$ | $\frac{-D^2+D+8}{2}$ |
| Common ground feature | Yes | Yes | Yes | Yes | Yes | Yes |




*(a)* *(b)* *(c)*

**Figure 6.** *Comparison of the proposed converter with other common high step-up DC-DC conveters: (a) Gain versus duty cycle; (b) Total voltage stress/$V_o$ versus gain; (c) $V_S/V_o$ versus gain.*

As shown in Table 2 and Figure 6(a)–(c), the voltage gain of the proposed converter is the same as that of [19]. Although both are not the highest among the compared designs, the proposed converter's voltage gain is very close to that of the converter in [11]. Notably, the voltage stress on the proposed converter is significantly lower than that of the converter in [11] and [19]. While the converters in [10] and [20] exhibit lower voltage stress than the proposed design, the proposed converter achieves a much higher voltage gain while operating at a lower duty cycle. This reduction in duty cycle results in lower stress on the active components, thereby enhancing both reliability and stability. Furthermore, compared to the converter in [12], the proposed design uses one fewer diode and one additional capacitor, yet it delivers a higher voltage gain and lower voltage stress. This leads to a more cost-effective solution, as fewer critical components are subjected to high stress, simplifying the design and reducing manufacturing costs.

## 6. Conclusion

This paper introduces the proposed converter, which provides several advantages, including a high voltage conversion ratio, minimized component stress, and reduced energy storage requirements. These attributes make the proposed converter particularly well-suited for integration with renewable energy systems, such as solar PV applications. The theoretical design of the proposed converter is outlined, and its efficiency is theoretically examined. Simulation verifications, when compared to theory, demonstrate consistency and align with the expected results. The comparison with other high step-up converters is shown. In the future, an experiment will be conducted to confirm all theoretical analyses and simulation results.

## Acknowledgments

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## Conflict of Interest

The authors declare no conflict of interest.

## Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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