JTE HCMUTE
ISSN: 2615-9740

JOURNAL OF TECHNICAL EDUCATION SCIENCE
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A New Buck-Boost Converter Configuration Reducing Current Stress on the Switch

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ARTICLE INFO

Received: 18/01/2025
Revised: 08/02/2025
Accepted: 20/06/2025
Published:

KEYWORDS

Buck-Boost Converter;
SEPIC Converter;
DC-DC Converter;
Non-Isolated;
Positive Output.

ABSTRACT

This paper presents a novel configuration for a DC buck-boost converter that mitigates current stress from inductors and capacitors on the switches during conduction states. Steady-state analysis, ripple current, voltage stress, and power loss evaluations have been conducted. Simulation and analytical results in buck and boost modes reveal that the proposed converter exhibits very low ideal load current overshoot for switches S1, S2, and diodes D1 and D2, even when the conversion ratio ranges from 0.2 to 2. This performance surpasses SEPIC and other analyzed configurations, contributing to reduced power losses and improved overall efficiency. Furthermore, performance experiments, including the impact of parasitic resistances, confirm that the proposed converter achieves the highest efficiency compared to other converters. These results demonstrate superior performance, reduced power losses, and extended lifespan, making the converter an optimal solution for power electronics and electrical applications. In addition, the converter features continuous input and output currents, making it particularly suitable for renewable energy applications such as photovoltaic systems, battery energy storage, and microgrid systems, where current continuity is essential for enhancing system stability and minimizing electromagnetic interference.

Doi: https://doi.org/10.54644/jte.2025.1816

1. Introduction

Renewable energy sources have become increasingly popular today due to the depletion of fossil fuel reserves and their environmental pollution. Renewable energy is the best solution for providing clean energy sustainably and without causing environmental pollution. It has many advantages and is starting to be widely used. The output power of renewable energy sources depends on weather and climate. These renewable energy sources, such as photovoltaic panels, require DC-DC converters to regulate the DC output voltage to match the load or storage devices, ensuring the voltage requirements for connection to a DC-AC converter for the power grid. DC-DC converters play an essential role to meet the voltage regulation requirements for diverse loads in the power grid, some of which require higher or lower voltage levels than the source voltage. These converters must have a simple structure, high efficiency, and high precision to meet the needs of voltage step-up and step-down [1]. The development of semiconductor technology since the early 19th century has facilitated the widespread use of DC-DC converters in power electronics [1], [2].

The DC-DC converter is an essential component in power conversion systems, allowing for the efficient conversion of one voltage level to another. It is widely used in renewable energy, electric vehicles, continuous power supplies, and microgrids. DC-DC converters are classified into two main types: isolated and non-isolated, based on the degree of electrical isolation between the input and output. Isolated converters use transformers to separate the source and load, enhancing safety but simultaneously increasing the cost and size of the device. Moreover, the leakage inductance of the transformer can cause voltage spikes, leading to stability issues [3], [4]. On the other hand, non-isolated converters are widely used due to their advantages of high efficiency, compact size, low cost, and low input current ripple. These characteristics make them suitable for low-power applications with simple structures and high economic feasibility [5], [6].

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Standard non-isolated DC-DC converter configurations in step-up or step-down applications include buck, boost, buck-boost, SEPIC, Ćuk, Zeta, and flyback converters. For renewable energy sources such as solar, wind, and biogas, the output power fluctuates continuously, leading to unstable voltage, which makes it challenging to meet the requirements of grid-connected inverters. Therefore, converters need to ensure the ability to adjust the output voltage flexibly, maintain low ripple levels, and reduce stress on semiconductor switches [7]. Among these options, SEPIC is preferred over flyback because it maintains an output voltage with the same polarity as the input and produces lower ripple current. However, the structural characteristics of SEPIC cause the semiconductor switch S1 (as shown in Figure 1) to be influenced simultaneously by the currents of inductor L1 and capacitor C1. This results in a high current stress on the switch, leading to power loss and elevated temperature, which reduces the circuit's efficiency and lifespan.

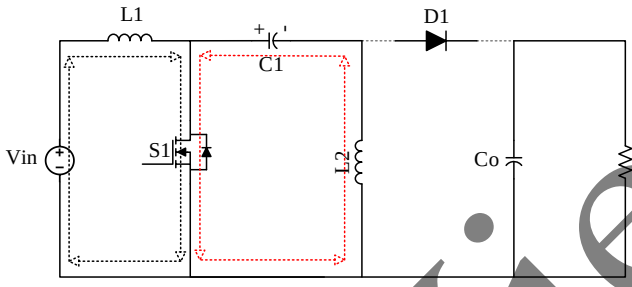

Figure 1. *The effect of current on the switch of the SEPIC converter*

This study proposes a new step-up/step-down configuration by restructuring the circuit with an additional switch and diode to prevent current from capacitor C1 from flowing through switch S1, thereby reducing the significant current stress on it.

2. Proposed topology

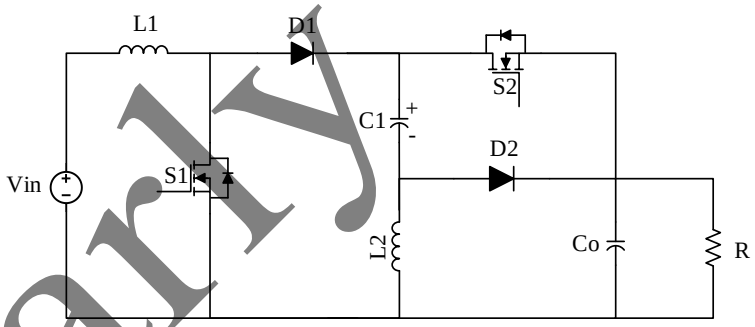

Figure 2. *The proposed converter*

The proposed converter, as illustrated in Figure 2, operating at a frequency of 50 kHz. The semiconductor switches S1 and S2 are synchronously controlled to turn on and off, while the diodes D1 and D2 remain reverse-biased during the activation of the switches.

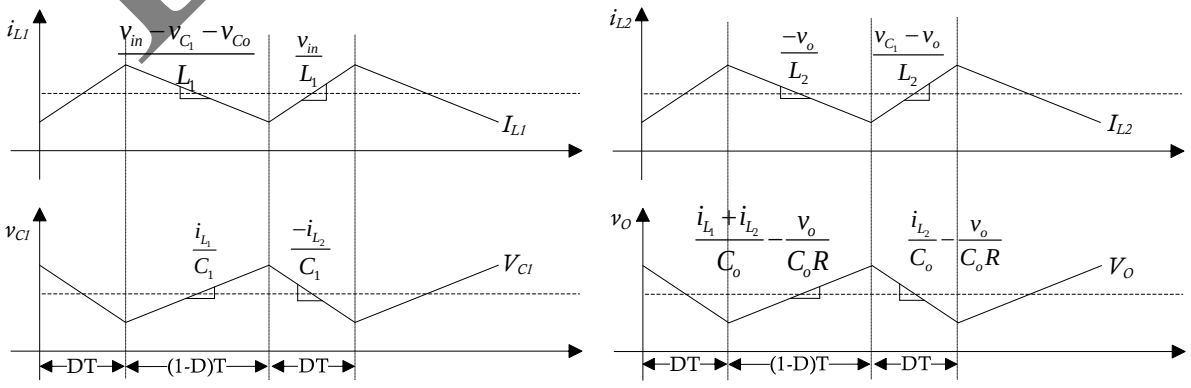

Figure 3. *Typical waveforms of the proposed converter in the time domain.*

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The converter operates in two main modes, assuming that the inductors and capacitors are designed with sufficiently large values to ensure continuous conduction mode (CCM). Under this condition, the voltages across capacitors C1, Co are considered constant. Notably, the current through inductor L1 maintains continuous input current supply in both operating modes, minimizing input current ripple. Simultaneously, the current through inductor L2 ensures a continuous output current waveform, improving output power quality. Details of the two operating modes of the converter will be presented in Sections 2.1 and 2.2.

2.1 Stage 1

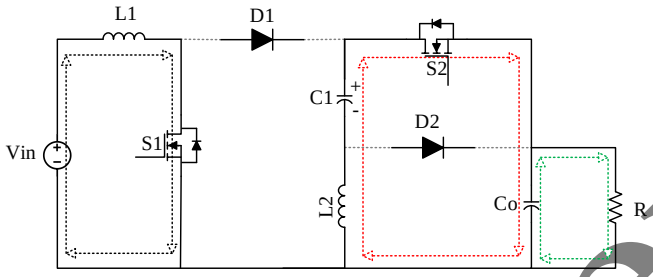

Figure 4. *Stage 1*

The switches S1, S2 are turned on for a duration corresponding to the duty cycle DT, as illustrated in Figures 3 and 4. At the same time, the diodes D1, D2 remain reverse-biased and do not conduct. During this stage, the input voltage Vin provides energy to inductor L1, while capacitor C1 is the energy source for inductor L2.

The voltage across capacitor C1 is equal to the voltage applied to diode D2, which indicates the voltage stress experienced by this diode. In the same way, the output voltage Vo corresponds to the voltage stress on diode D1. The circuit operation during this stage can be described using differential equations, as shown in Equation (1).

$$\begin{cases} L_1 \dfrac{di_{L_1}}{dt} = v_{in} \\ L_2 \dfrac{di_{L_2}}{dt} = v_{C_1} - v_O \\ C_1 \dfrac{dv_{C_1}}{dt} = -i_{L_2} \\ C_O \dfrac{dv_o}{dt} = i_{L_2} - \dfrac{v_O}{R} \end{cases} \quad (1)$$

2. 2 Stage 2

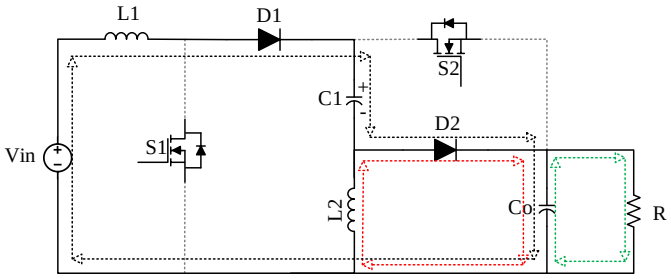

Figure 5. *Stage 2*

During the time interval (1−D)T, as illustrated in Figures 3 and 5, the switches S1 and S2 are turned off, while the diodes D1 and D2 are forward-biased and conduct. In this phase, the input voltage Vinand

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the energy stored in inductor L1 supply energy to capacitor C1 through diodes D1 and D2. Simultaneously, inductor L2 transfers its stored energy to the output capacitor Co via diode D2.

The differential equations describing the relationship between voltage and current during this stage can be derived and represented in Expression (2).

$$\begin{cases} L_1 \dfrac{di_{L_1}}{dt} = v_{in} - v_{C_1} - v_O \\ L_2 \dfrac{di_{L_2}}{dt} = -v_O \\ C_1 \dfrac{dv_{C_1}}{dt} = i_{L_1} \\ C_O \dfrac{dv_o}{dt} = i_{L1} + i_{L_2} - \dfrac{v_O}{R} \end{cases} \quad (2)$$

2. 3 Voltage Conversion Ratio

In steady-state conditions, the inductors are elements with zero reactance, meaning the average voltage across them during a working cycle is zero. By applying the Volt-Second balance principle from Equations (1) and (2), the relationship is obtained and expressed in Equation (3).

$$\begin{cases} DV_{in} + (1-D)(V_{in} - V_{C_1} - V_O) = 0 \\ D(V_{C_1} - V_O) + (1-D)(-V_O) = 0 \end{cases} \quad (3)$$

From Equation (3), the voltage across capacitor C_1 and C_0 are determined as (4) and (5), respectively.

$$V_{C_1} = \frac{V_{in}}{1-D^2} \quad (4)$$

$$V_O = \frac{DV_{in}}{1-D^2} \quad (5)$$

Therefore, the proposed converter's voltage conversion ratio (M) can be determined by (6).

$$M = \frac{V_O}{V_{in}} = \frac{D}{1-D^2} \quad (6)$$

3. Simulation results

To assess the performance of the proposed converter, this paper conducts a detailed analysis and compares its current-handling capability with other common buck-boost configurations, including the SEPIC converter and designs described in previous studies [8], [9]. The analysis focuses on energy efficiency and factors related to stability and reliability during operation.

Furthermore, circuit components are numbered in the order of appearance to facilitate observation and verification in simulations, and the ideal component models available in PSIM software are employed. This approach makes it easier to identify and track each element within the system, as illustrated in Figure 6. A 48VDC voltage source is used as the test input to ensure objectivity and consistency in measurements. Component parameters include a 47 µF capacitor, a 0.4 mH inductor, diodes and MOSFETs of the same type, a 15 Ω load resistor, and a 50 kHz switching frequency applied across all converters. This experimental setup ensures equivalent conditions, providing a solid basis for accurate evaluation and fair performance comparison of the converter configurations.

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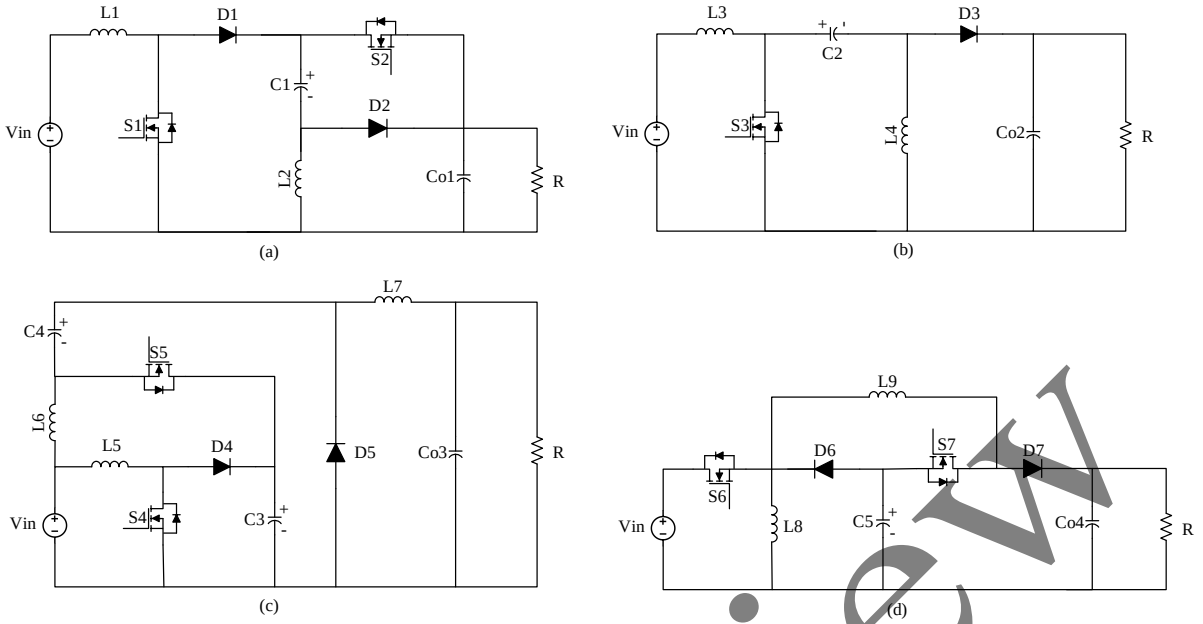


Figure 6. *(a) Proposed converter, (b) SEPIC converter, (c) Converter according to study [8], (d) Converter according to study [9].*

3.1. Stress current on the switches and diodes in the buck mode

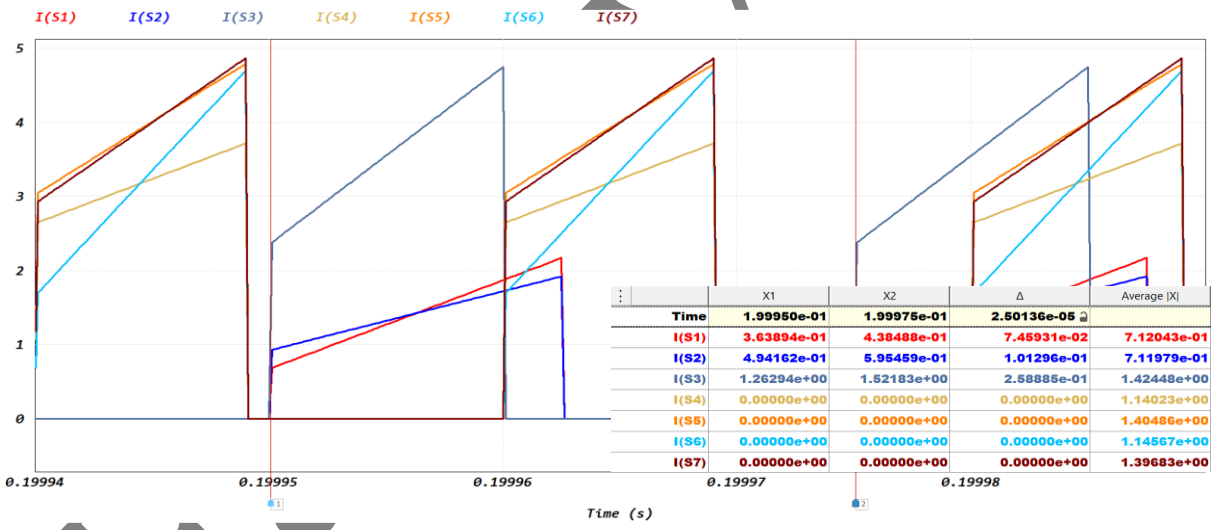


Figure 7. *Current through the switches of the converters in buck mode.*

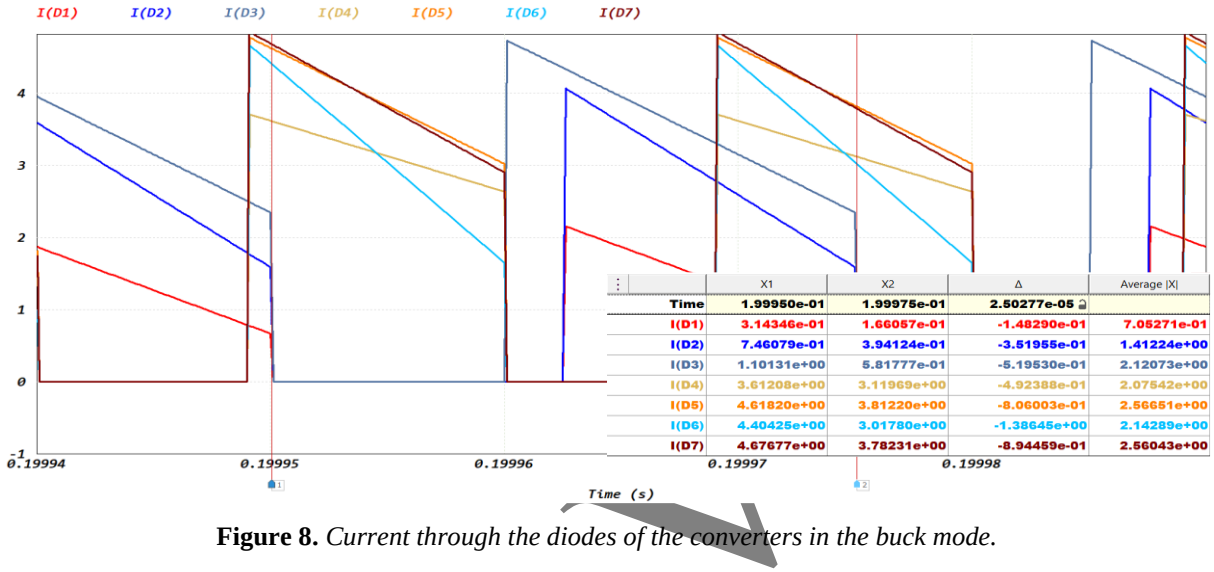
The current waveform of the converters operating in buck mode is illustrated in Figure 7, with a transformer ratio of M=0.66 (corresponding to an output voltage of 32 VDC). The proposed converter demonstrates superior performance, with the average current through switches S1 and S2 reaching 0.71A, which is 33.28% of the load current under ideal conditions. In contrast, the SEPIC converter shows an average current of 1.42A through switch S3, accounting for the highest percentage of 66.56%.

For the Quadratic converter mentioned in the study [8], the average current through switch S4 is equivalent to the current through switch S6 of the converter in the paper [9], with a ratio of 53.43%. Similarly, the average current through switches S5 and S7 of these two converters is approximately 1.4A, accounting for 65.62%.

In summary, in buck mode, the proposed converter exhibits significantly lower current stress on the switches, resulting in higher operational efficiency and contributing to the extended lifespan of the semiconductor switches.

Figure 8 illustrates the current through the diodes in the converter configurations. The average current through diode D1 for the proposed converter is 0.7A. Meanwhile, the current through diode D2, influenced by the currents of inductors L1 and L2 during phase 2, has a relatively high average value of 1.41A.

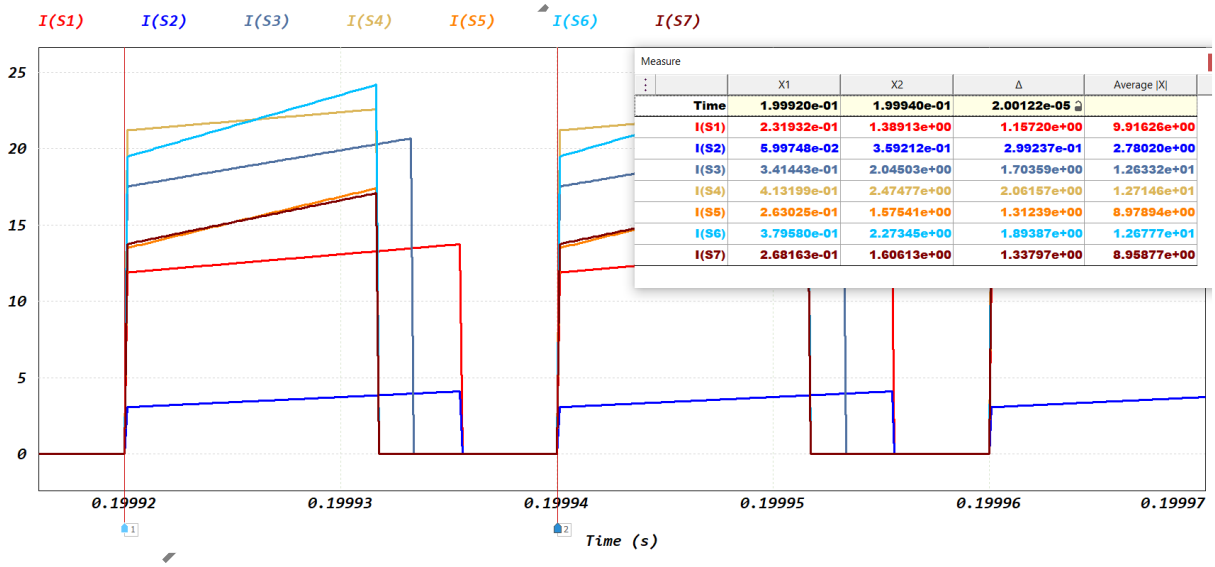
Compared to other converters, the current through diode D2 in the proposed converter is approximately 45% lower than the peak current observed through diodes D5 and D7 in studies [8] and [9], respectively. In those studies, the average current through diodes D4 and D6 is 2.07A and 2.14A, respectively.



	X1	X2	Δ	Average |X|
Time	1.99950e-01	1.99975e-01	2.50277e-05	
I(D1)	3.14346e-01	1.66057e-01	-1.48290e-01	7.05271e-01
I(D2)	7.46079e-01	3.94124e-01	-3.51955e-01	1.41224e+00
I(D3)	1.10131e+00	5.81777e-01	-5.19530e-01	2.12073e+00
I(D4)	3.61208e+00	3.11969e+00	-4.92388e-01	2.07542e+00
I(D5)	4.61820e+00	3.81220e+00	-8.06003e-01	2.56651e+00
I(D6)	4.40425e+00	3.01780e+00	-1.38645e+00	2.14289e+00
I(D7)	4.67677e+00	3.78231e+00	-8.94459e-01	2.56043e+00

Figure 8. *Current through the diodes of the converters in the buck mode.*

3.2. Stress current on the switches and diodes in the boost mode



Measure

	X1	X2	Δ	Average |X|
Time	1.99920e-01	1.99940e-01	2.00122e-05	
I(S1)	2.31932e-01	1.38913e+00	1.15720e+00	9.91626e+00
I(S2)	5.99748e-02	3.59212e-01	2.99237e-01	2.78020e+00
I(S3)	3.41443e-01	2.04503e+00	1.70359e+00	1.26332e+01
I(S4)	4.13199e-01	2.47477e+00	2.06157e+00	1.27146e+01
I(S5)	2.63025e-01	1.57541e+00	1.31239e+00	8.97894e+00
I(S6)	3.79580e-01	2.27345e+00	1.89387e+00	1.26777e+01
I(S7)	2.68163e-01	1.60613e+00	1.33797e+00	8.95877e+00

Figure 9. *Stress current on the switches and diodes in the boost mode.*

With a voltage conversion ratio of M=2 used as the experimental model for the boost mode, Figure 9 illustrates the current through the switches of the converters. For the proposed converter, the average current passing through switches S1 and S2 is 9.91 A and 2.78 A, respectively. These values represent 154% and 43.43% of the ideal load current. The SEPIC converter shows the highest average current through switch S3, reaching 12.63A (197.34%). The average current through switch S4 of the converter in the study [8] is almost equivalent to the current through switch S6 of the Quadratic converter in the document [9], reaching 198.59%. Similarly, the average current through switches S5 and S7 of these two converters is approximately 8.97A, representing 140.15%.

Overall, the proposed converter shows significantly lower current usage through switch S2 in the boost mode. However, due to its specific structure with a first-degree function in the denominator, this converter is more suitable for step-down applications. When operating in boost mode, switch S1 needs to remain active longer than in other converters, leading to a current through S1 that is 13.85% higher than the current through switches S5 and S7 in the studies [8], [9].

Figure 10 illustrates the current through the diodes of the converters. With the proposed converter, the average current through diode D1 is 2.9A, while the current through diode D2 reaches 3.71A. Compared to other converters, the current through diode D2 in the proposed converter is 40.34% lower than the maximum current through diodes D4 and D6 [8]. The average current through diodes D5 [8] and D7 [9] is approximately 6.46A.

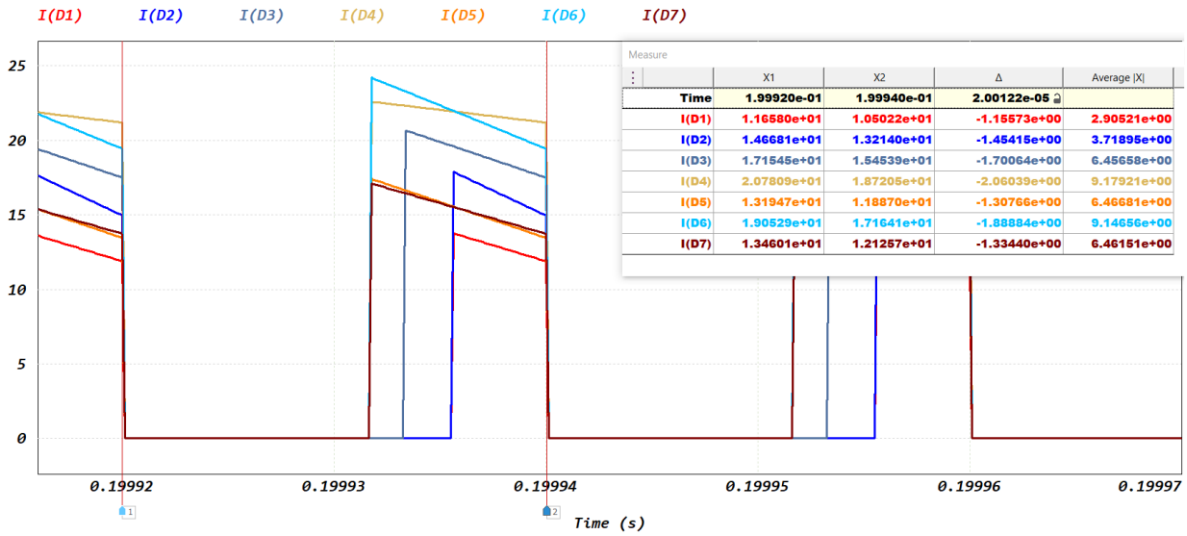


Figure 10. *Current through the diodes of the converters in boost mode.*

Figures 11a and 11b illustrate the experimental results of the current over-load factor in ideal conditions for the power switches and diodes within the transformer ratio range from 0.2 to 2. The results show that the proposed converter maintains the current through switch S2 at no more than 0.5 times the load current, while switch S1 reaches a peak of 1.55 times the load current. The current through diodes D1 and D2 only reaches a maximum of 0.84 times the load current, significantly lower than the SEPIC converters and those studied in [8], [9]. These results confirm the converter's superior ability to optimize current, contributing to improved efficiency and prolonged system lifespan.

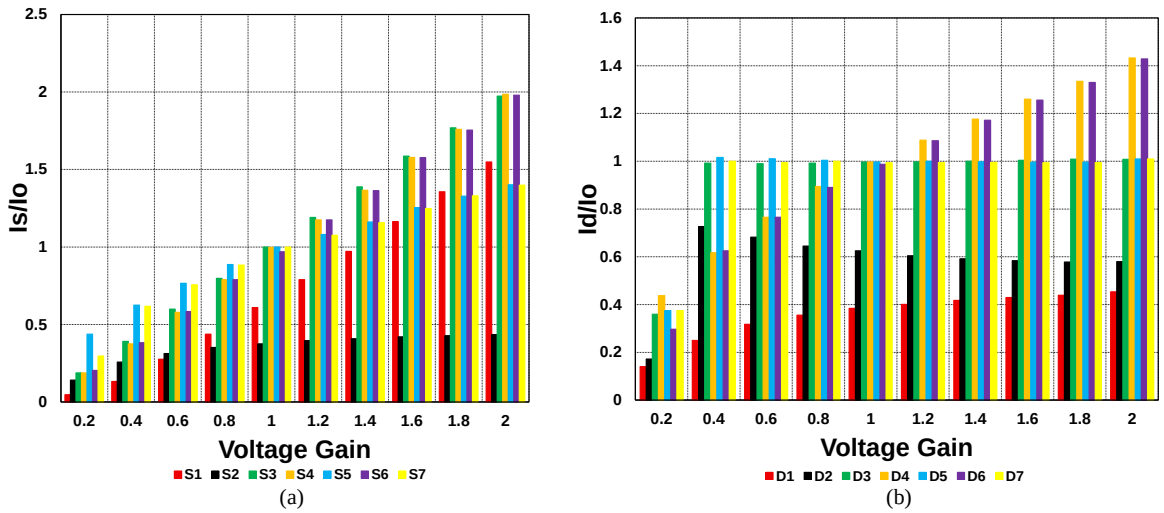


Figure 11. *Overload current ratio with respect to transformer ratio for the components of the proposed converter, SEPIC, and [8], [9]: (a) Power switches, (b) Diodes.*

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To assess the detailed performance and stable operating range of the proposed converter, an experiment was conducted by simulating parasitic resistances on key components such as inductors, capacitors, and diodes. In this experiment, the parasitic resistances were set at ratio levels of 0.001, 0.002, and 0.003 relative to the load value. This method not only helps to evaluate the overall performance but also clearly identifies the impact of parasitic factors on the stability and operational capability of the converter under different conditions, thereby informing the audience about potential challenges. Through this, the converter's ability to operate efficiently in real-world environments is comprehensively validated. The parameters of the converters were consistently configured to maintain objectivity. The capacitors used had a value of 47 µF, the inductors were set to 0.4 mH, the resistive load was established at 15 Ω, the supply voltage for the converters was fixed at 48 VDC, and a 50 kHz switching frequency applied across all converters.

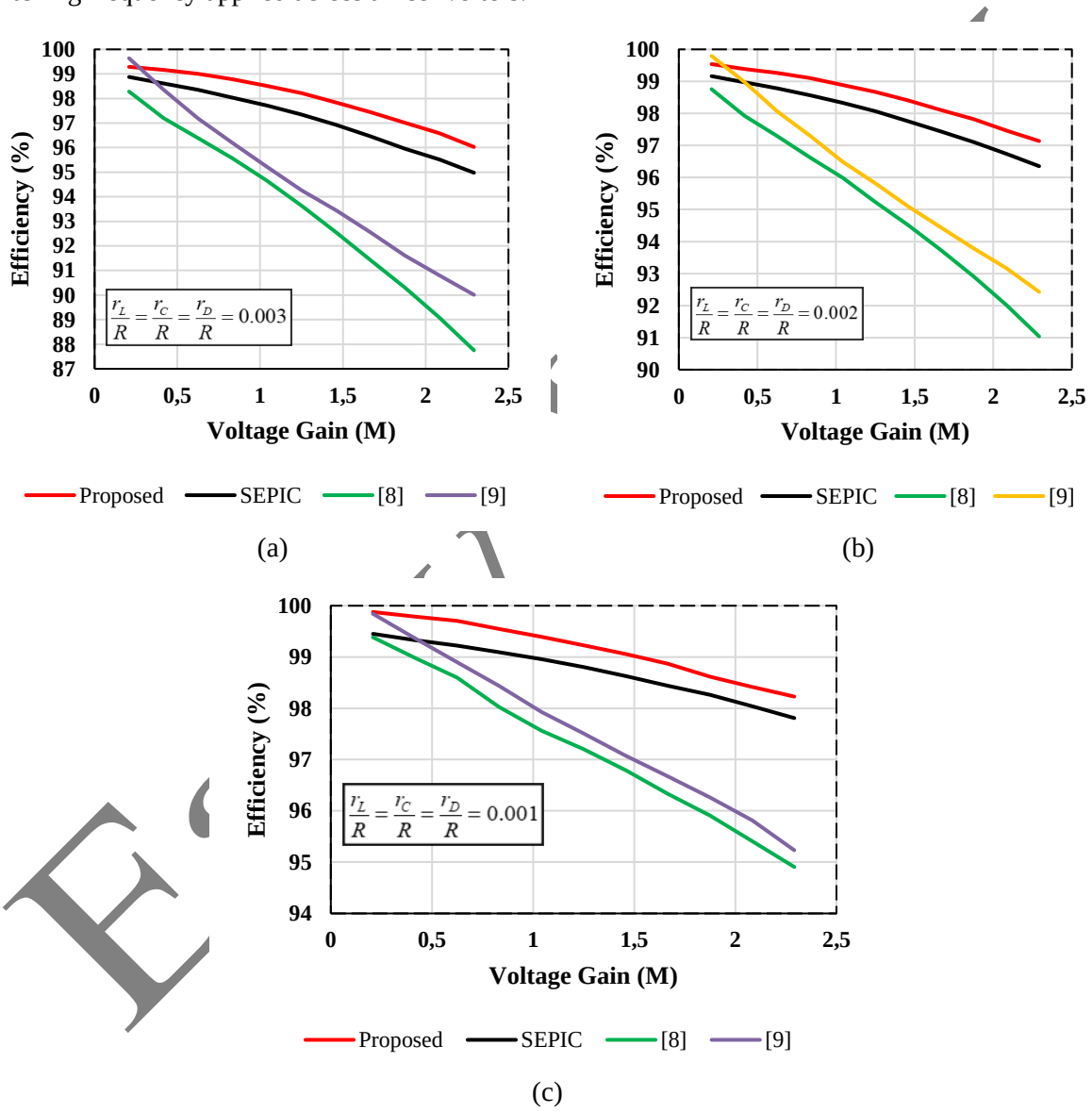

Figure 12. *Efficiency of the converters with parasitic resistance proportional to the load value: (a) 0.03, (b) 0.02, (c) 0.01*

Figure 12 clearly illustrates parasitic resistance's impact on converters' performance. In Figure 12a, with the ratio of parasitic resistance to load resistance at 0.03, the Quadratic converter [8] achieves a maximum efficiency of only 98.28%. It operates stably within a voltage ratio range of 0.2 to 2.29, the lowest among the converters. The converter from the study [9] performs better, with a peak efficiency of 99.64%. However, it gradually loses its advantage as efficiency decreases rapidly, falling below the

proposed converter in the voltage ratio range of 0.4 to 2.29. In contrast, the proposed converter and the SEPIC maintain stable operation over a broader range, with the proposed converter achieving a maximum efficiency of 99.29%.

Figure 12b further confirms the advantages of the proposed converter, with an efficiency of 99.54%, surpassing the SEPIC by 0.38% and the converter in [8] by 0.78%, even though these configurations also improve their operational stability ranges. For the configuration of the converter in the study [9], it dominates in the initial stage with an efficiency of up to 99.79%. However, it declines rapidly and becomes less stable than the proposed converter.

Figure 12c shows that when parasitic resistance's impact decreases, all converters' efficiency exceeds 94%. Nevertheless, the proposed converter remains the leader with an impressive efficiency of 99.88%, demonstrating exceptional performance in minimizing losses and optimizing efficiency.

4. Conclusions

The paper proposes a novel non-isolated buck-boost DC-DC converter with the capability to reduce current stress on the switches. Results from theoretical calculations, simulations, and experiments validate that the proposed converter demonstrates superior current utilization and efficiency performance. In buck mode, the current through the switches only accounts for 33.28% of the load current, significantly lower than SEPIC (66.56%) and Quadratic (65.62%), leading to improved operational efficiency and extended component lifespan.

The efficiency of the converter reaches a maximum of 99.88% when the impact of parasitic resistance is reduced to 0.001, outperforming SEPIC by 0.43% and exceeding the efficiency of the Quadratic converters in studies [8] and [9] by 0.5% and 0.04%, respectively. Even with parasitic resistance increasing to 0.003, the efficiency remains at 99.29%. These results demonstrate the converter's ability to optimize current flow and minimize losses, enabling more efficient and stable operation than other configurations. These findings confirm that the proposed converter is particularly well-suited for applications that require buck mode operation with high efficiency and low current through semiconductor components. This includes power electronics systems used in renewable energy applications, such as solar energy systems and battery management, where high efficiency and component durability are essential. Additionally, the converter is ideal for systems that aim to minimize the effects of parasitic elements, ensuring stable and sustainable operation.

Acknowledgments

This research was supported by the Renewable Energy & Power System Laboratory (C201), Industrial Power System Control Laboratory (C402) at Ho Chi Minh City University of Technology and Education, Vietnam.

Conflict of Interest

The authors confirm that there are no conflicts of interest. The final draft was read and approved by each author.

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