JTE HCMUTE
ISSN: 2615-9740

JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Education
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

Dedicated SoC Peripheral Design for Power Control Applications on the Xilinx Ultrascale+ Platform

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ARTICLE INFO

Received: 22/04/2025
Revised: 09/09/2025
Accepted: 30/09/2025
Published online: 09/10/2025

KEYWORDS

High-performance control;
Dynamic configuration;
ePWM (enhanced PWM);
Hardware-software co-design;
Multi-level inverter.

ABSTRACT

This paper presents the design, implementation, and validation of a high-performance, configurable control architecture exploiting the heterogeneous computing fabric of the Xilinx UltraScale+ MPSoC XCZU3CG. Targeting demanding real-time applications like multi-level power converters, the core contribution is an optimized hardware/software partitioning strategy. We detail the tight integration of the ARM Cortex-A53 Processing System (PS) with custom parallel processing elements synthesized within the Programmable Logic (PL). The implemented VHDL-based PL architecture features multiple independent controller modules, achieving significant parallelism and providing 176 precisely controlled ePWM outputs crucial for fine-grained actuation. A key design element is the robust PS-PL AXI interface, facilitating efficient run-time parameter configuration of hardware controllers from the PS, enhancing operational flexibility. The design methodology prioritized deterministic low-latency performance alongside optimized PL resource utilization. The register interface intentionally mirrors familiar DSP conventions to ease system integration. Experimental results successfully validate the MPSoC architecture's functional correctness and performance metrics, demonstrating its effectiveness for substantially accelerating the design cycle for complex embedded control systems, The system-on-chip (SoC) was validated using a pulse generation configuration across ten sets of T-Type three-level inverter configurations, resulting in a total of 120 pulse-width modulation (PWM) outputs.

Doi: https://doi.org/10.54644/jte.2025.1881

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1. Introduction

Contemporary embedded systems for power converter management are increasingly demanding in terms of parameters and features. Typically, digital signal processors (DSPs) and microcontrollers are employed to generate control signals. However, these controllers encounter limitations concerning computational complexity and the number of PWM signals they can manage. Complex control algorithms necessitate substantial computation time. For straightforward control requirements, where custom parameters can be configured via software and adapted to various applications, DSPs are suitable. Nevertheless, for more intricate applications, DSPs prove inadequate when high-performance devices with substantial computing power are available [1-2]. In such instances, FPGAs are preferable due to their hardware programmability and highly customizable specifications. A device capable of customizing both hardware and software are essential for power conversion control research. Furthermore, FPGAs can execute complex algorithms and parallel computations using logic circuits [3]. The capability to configure hardware via logic blocks facilitates the design of specific modules for power converter control [4]. To fully leverage the benefits of FPGA-based systems, developers frequently employ Hardware Description Languages (HDL) or Xilinx System Generator (XSG) [5]. Although XSG simplifies development through graphical design, it often produces inefficient HDL code and offers a more limited set of functional blocks compared to MATLAB. Contemporary FPGAs incorporate dedicated hardware processor cores, which enable efficient sequential processing, support for operating systems, and peripheral interfacing. Implementing FPGA architectures grounded in Digital Signal

Processing (DSP) principles significantly enhances the ability to manage numerous enhanced Pulse Width Modulation (ePWM) signals. FPGAs are inherently designed for extensive parallelism, rendering them ideal for applications necessitating synchronized control across multiple PWM channels [6]. FPGA-based synchronization mechanisms ensure precise alignment even with a substantial number of ePWM blocks. Regarding timing performance, FPGAs can achieve a time resolution as fine as 41.3 ps using 14-bit Digital PWM (DPWM) with triangle waveforms [7]. Moreover, advanced techniques such as Variable Clock Phase Shifting can reduce this resolution to below 5 ps [8]. Given that switching frequencies can reach up to 2 MHz—equivalent to an 11-bit DPWM—systems can attain effective performance without necessitating excessively high bit-depths [9]. As multi-level inverter architectures expand from three to as many as 21 levels, the number of required power switches and corresponding PWM control signals increases significantly [10]. In this context, Pulse Width Modulation techniques are crucial. Among the most widely adopted are third harmonic injection PWM, space vector PWM, and sine-triangle PWM, particularly in applications involving three-level T-type inverters (3LT2I) [11]–[13].

This paper presents a reconfigurable FPGA-based System-on-Chip (SoC) architecture designed for power electronics control. The system enables dynamic, self-programmable configuration of inverter outputs using an integrated ARM processor, without requiring full FPGA reconfiguration. Built on the Xilinx UltraScale+ platform, the architecture includes dedicated peripheral hardware and supports high-level programming in C. The SoC features four ARM Cortex-A53 cores and two Cortex-R5 real-time cores, which interface with peripherals via a 12.8 Gbps AXI4 interconnect for efficient, low-latency control.

The architecture supports up to 176 PWM outputs for precise control of inverters, controlled rectifiers, and multi-level converter systems. Handshake mechanisms between processing cores and PWM units allow synchronized switching, improving timing accuracy and system reliability. This design offers a scalable and flexible solution for embedded power systems, enabling real-time control and rapid prototyping within a unified hardware-software environment, making it suitable for applications in renewable energy, industrial automation, and electric drive systems.

2. Hardware Architecture and Implementation

2.1. FPGA-Based SoC for power control

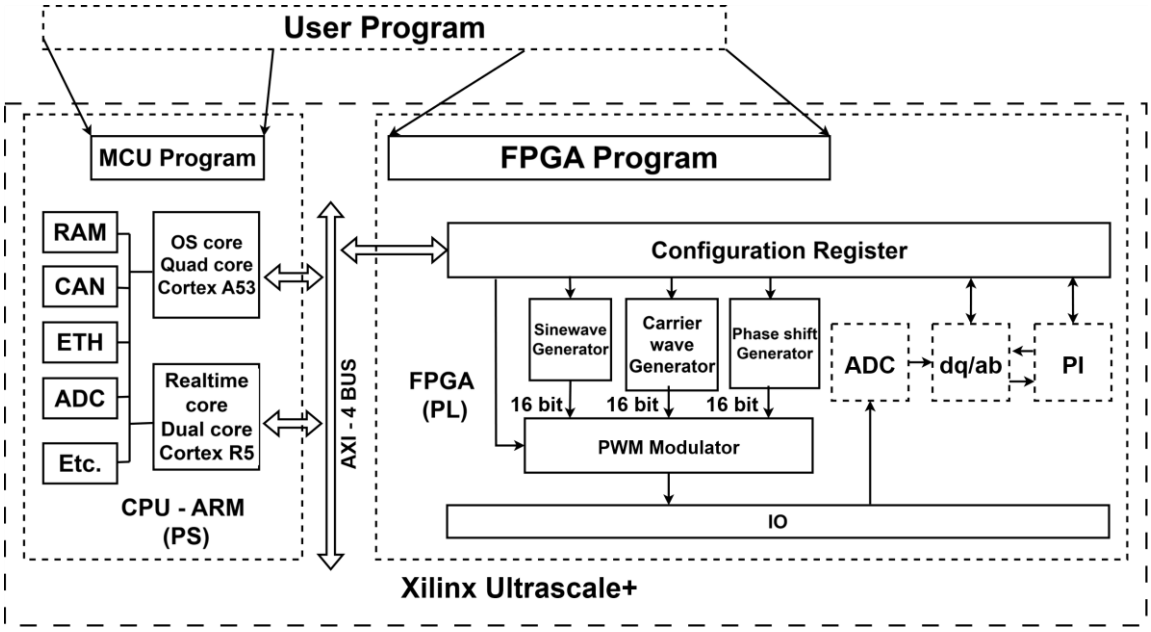

Figure 1. *The architecture of FPGA-Based SoC.*

The proposed System-on-Chip (SoC) architecture integrates dedicated power control logic blocks within the FPGA fabric, enabling efficient and flexible control of power electronic systems. As illustrated in Figure 1, the FPGA includes pre-programmed specialized logic modules, such as sine wave

generators, sawtooth waveform generators, and PWM controllers. Each module is configurable via a dedicated set of memory-mapped registers, which are accessible by user applications written in high-level languages such as C or C++. A custom compiler framework integrates precompiled VHDL modules with the user's software, generating a combined bitstream suitable for both the FPGA and the ARM processing cores. In this architecture, the FPGA acts as a dedicated peripheral for executing time-sensitive PWM operations, while the ARM Cortex processors handle high-level control, configuration, and communication tasks. The ARM cores connect with various system peripherals, such as RAM controller, ADC, and monitor interface. This architecture enables the FPGA to simulate enhanced PWM (ePWM) modules, akin to those in conventional DSP systems. Furthermore, the available logic resources can be configured to execute sophisticated power control algorithms like the Park (dq0) Transform and Space Vector Modulation (SVM). The extensive FPGA resources facilitate the creation of numerous specialized power control modules, achieving exceptionally high execution speed and determinism. Operating principle of ePWM block.

In digital signal processors (DSPs), the enhanced Pulse Width Modulation (ePWM) block functions as a flexible module capable of supporting various tasks. In power electronics, its main role is to produce PWM control waveforms for operating switching devices. The ePWM block includes an integrated prescaler that lowers the input clock frequency, allowing for adaptable carrier frequency adjustments. A Period Register sets the counter's maximum value, which dictates the total PWM period. The Compare Register holds duty cycle values for two output channels, typically known as channels A and B. An Action Qualifier module specifies the output's behavior when the counter matches the compare values. The Dead-Band Generator adds a delay between complementary outputs to avoid shoot-through in power switches. The PWM Chopper adjusts the pulse width to provide additional control features, while the Trip Zone module instantly disables outputs in the event of fault conditions. Furthermore, synchronization ports allow multiple ePWM blocks to operate in phase or with defined timing relationships. The complete architecture of the ePWM module, as implemented in the TI TMS320F28335 DSP, is illustrated in Figure 2.

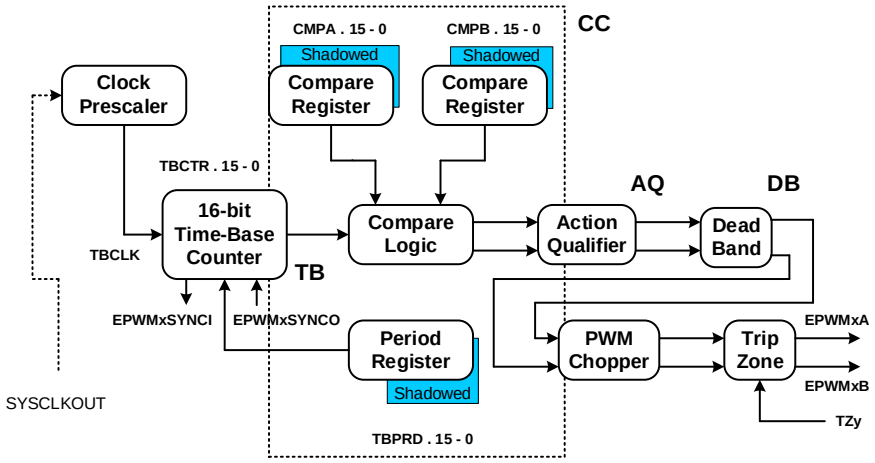

Figure 2. *ePWM Block of DSP.*

The ePWM peripheral is specifically designed for generating the high-resolution PWM waveforms required for controlling power switching devices. Central to its operation is the Time-Base (TB) module, whose counter produces the carrier waveform, typically configured for triangular (up/down count) or sawtooth (up or down count) profiles. The switching frequency is precisely determined by the value loaded into the Time-Base Period Register (TBPRD), which establishes the counter's rollover point. Duty cycle control is achieved by comparing the instantaneous Time-Base Counter (TBCTR) value against the active Compare Register (e.g., CMPA/CMPB), which holds the desired reference level for that PWM cycle. The Action Qualifier (AQ) module interprets the comparison events (e.g., TBCTR = CMPA on up-count, TBCTR = Zero) and dictates the corresponding state transitions (set high, clear low, toggle) on the PWM output pins. This event-driven, modular design provides significant flexibility, enabling the synthesis of complex and customized PWM patterns essential for various power electronics control topologies.

2.2. Developing an FPGA-based ePWM Controller

By examining the DSP's ePWM block diagram, it becomes evident that the ePWM block is composed of two separate parts: the counter block, which is tasked with generating the carrier signal, and the PWM block, which is responsible for creating the PWM output. As a result, Figure 2 depicts the design of the counter block.

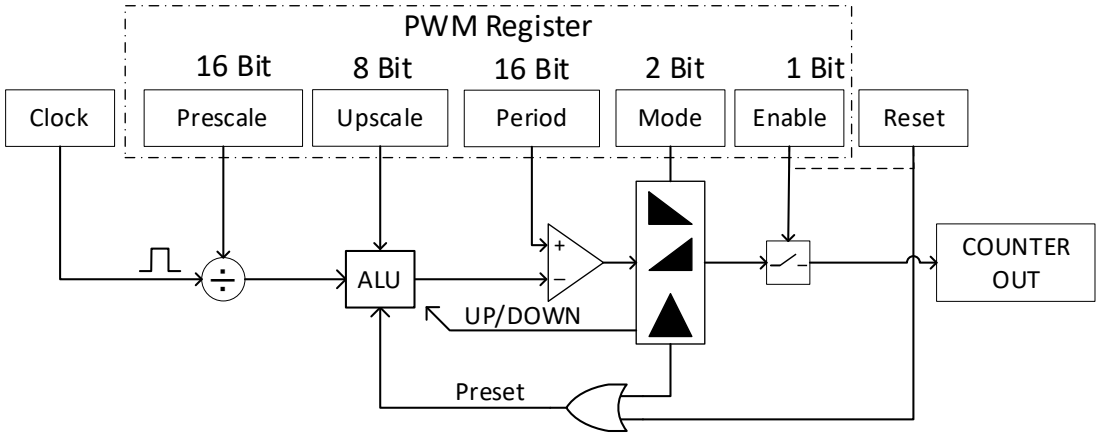

Figure 3. *Logic level design for counter block.*

Figure 3 illustrates that the Counter block consists of essential elements such as the clock Prescale, Period Register, and Time-base Counter. The Mode Register manages the input clock, which dictates whether the counter operates in an up, down, or up/down mode, allowing for the creation of a precisely controlled carrier waveform.. The Arithmetic and Logic Unit (ALU) calculates the next counter value based on the current state, ensuring accurate progression of the time base. The Upscale Register is employed to accelerate the counter from the base clock, thus increasing the carrier speed to achieve higher switching frequencies, which is essential for high-performance applications. The Counter block utilizes 178 Lookup Table (LUT) slices and 34 Flip-Flops (FF), optimizing logic density and performance. The switching frequency for a counter of fixed bit-width is determined by the relationship presented in Equation (1), which defines the timing characteristics necessary for achieving high-resolution, reliable PWM control in power electronics.

$$F_{SW} = \frac{F_{input} \times S}{p \times 2^{n-\sqrt{L-1}+k}} \quad (1)$$

Where:

F_{SW} : desired switch frequency

F_{input}: Frequency of Clock PLL

P: Prescale

S: Step size

L: Number of Voltage level

n: data width

k: mode select (up-down: 1, up or down: 0).

Figure 4 details the architecture of the implemented PWM module. This hierarchical design incorporates essential sub-modules, including Compare logic with its associated register, an Action Qualifier defining output state transitions, Dead-Band generation logic, a PWM Chopper unit for high-frequency modulation capabilities, and Trip-Zone logic for fault protection. Critically, integrated dead-time compensation, leveraging the methodology presented in [14], has been incorporated to preclude shoot-through conditions, which is particularly vital for reliably driving the targeted multi-level inverter topologies. The module achieves a 16-bit duty cycle resolution, providing fine-grained control, while its synthesized footprint utilizes 73 LUT slices on the target FPGA platform.

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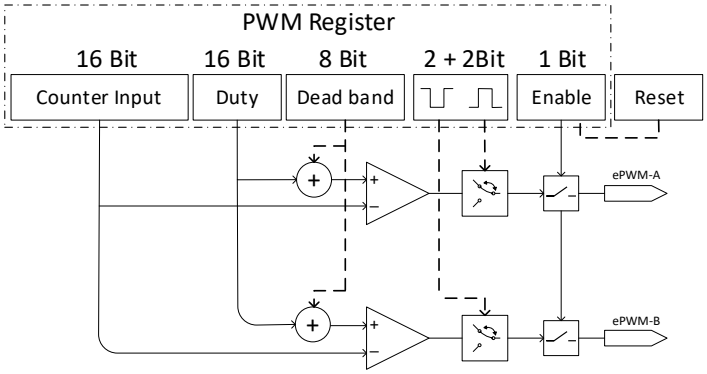

Figure 4. *Logic level design for PWM Block.*

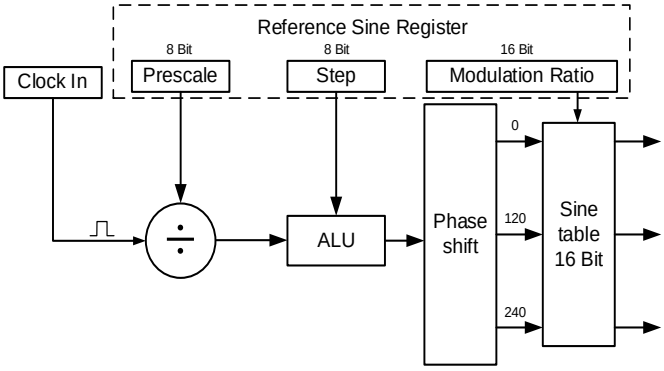

Figure 5. *Logic level design for referent wave generator*.

Figure 5 illustrates the architecture of the reference sine waveform generator, commonly implemented as a Numerically Controlled Oscillator (NCO). At its core, a counter block serves as a phase accumulator. The accumulator's output directly addresses a sine Look-Up Table (LUT), translating the accumulating phase angle into corresponding amplitude samples. The precise output frequency of this synthesized sine wave is dictated by the phase increment value provided to the accumulator, the calculation of which is specified in equation (2).

$$F_{sine} = \frac{F_{clk} \times stepsize}{P_{pre} \times 2^n} \tag{2}$$

Where:

F_{clk}: Carry waveform frequency

P_{pre}: Clock prescale

stepsize: stepsize lookup table

n: data width.

To streamline the hardware design and avoid processing negative numbers downstream, the sine Look-Up Table is pre-computed to store amplitude values directly in an N-bit unsigned (offset binary) format. Rather than storing values centered around zero (e.g., [−M,+M]), the LUT contains values mapped to the range [0,2M] by incorporating the necessary DC offset during generation. This design choice eliminates the need for a separate level-shifting stage at the output. The function below describes the mapping applied to generate these LUT entries.

$$f(k) = 2^{n-1} \times sin\left(\frac{k \times 2\pi}{2^n}\right) + 2^{n-1} \tag{3}$$

Where:

f(k): output of carry wave generator

n: data width

k: value of counter lookup

2.3. Implementation of ePWM Control for Multi-Level Systems

To confirm the setup of the System on Chip (SoC) model operating in 3LT2I mode, the author has arranged a total of 120 ePWM output inverter registers, which form nine inverters. The output waveforms from these nine controllers, corresponding to the 120 PWM outputs, were validated using both simulation and experimental approaches. The control signal from the SoC and power components is configured to 3LT2I to verify the output voltage waveform on the load.

Figure 6 depicts the operation mode of a 3-level inverter, which necessitates the use of two ePWM blocks functioning in handshake mode. The carrier signal is divided into two segments, with MSB=0 and MSB=1, both utilizing the same comparison signal.

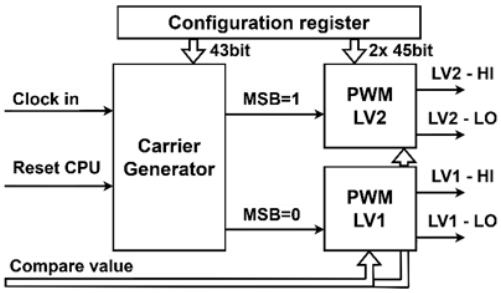

Figure 6. *Unit level design ePWM running handshake mode.*

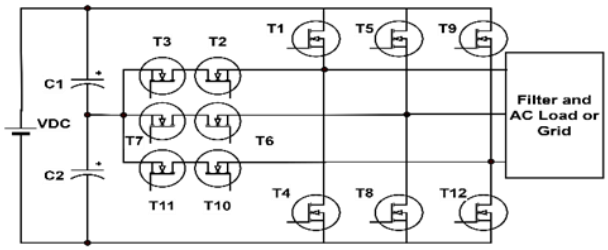

Figure 7. *3-Level T-Type Inverter.*

The control signals T1, T2, T3, and T4 are responsible for managing a single phase of the 3-level inverter depicted in Figure 7. This setup results in an ePWM block that utilizes 270 LUTs and 34 FFs in total. The T-type Inverter, employing a three-level topology, can produce three distinct voltage levels at its output. When switches T1 and T2, T5 and T6, and T9 and T10 are engaged, the output voltage reaches +VC. Activating switches T2 and T3, T6 and T7, and T10 and T11 results in an output voltage of 0. Similarly, the voltage drops to –VC when switches T3 and T4, T7 and T8, and T11 and T12 are activated. The number of the switches corresponds to Figure 7.

The T-Type Inverter, illustrated in Figure 7, operates using the ePWM control signal. This configuration utilizes a single carrier and enhances the waveform by altering the most significant bit (MSB) without the need for adder blocks, thus reducing delays in computation blocks. As a result, six carriers with two different amplitudes are produced for input into the PWM blocks, as shown in Figure 6. The three sine wave generator blocks are shifted by 120 degrees to create the reference waveform. Furthermore, a separate counter is used to modify the frequency of the desired reference wave.

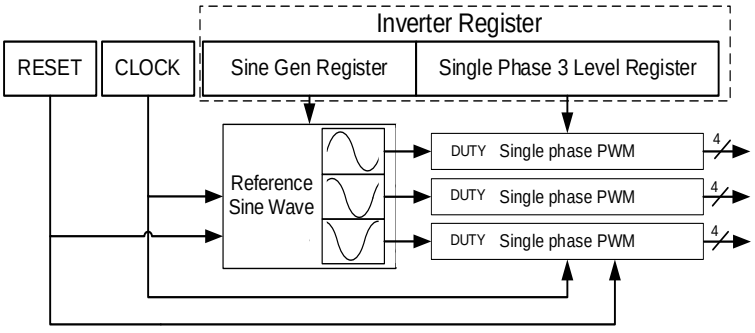

Figure 8. *Architecture level design of 3 level 3 phase inverter.*

Figure 8 presents the completed controller architecture for the three-level 3 phase inverter, implemented on the Xilinx Zynq UltraScale+ MPSoC XCZU3EG platform. The controller demonstrates highly efficient resource utilization, employing only 889 Look-Up Tables (LUTs) (1.69%), 558 Flip-Flops (FFs) (0.55%), 1.5 Block RAMs (BRAMs) (1.07%), and 6 Digital Signal Processing (DSP) slices (2.73%). This suggests that the implementation of six enhanced PWM (ePWM) blocks—yielding twelve PWM outputs—necessitates minimal hardware overhead. The modular and parameterizable architecture

further facilitates scalability, allowing designers to modify the number of ePWM units in accordance with the desired voltage level in multi-level inverter configurations. The XCZU3EG's integration of high-performance programmable logic and ARM Cortex-A53 cores renders it particularly suitable for advanced digital control in power electronics applications, ensuring both flexibility and real-time responsiveness within the programmable system-on-chip (SoC) environment.

The SoC can control A 21-level inverter could use the 176 ePWM signals to control up to 5 phases simultaneously, with fine-grained control over each switch in each phase. In the case of a multi-level rectifier PFC, the system could use 176 ePWM outputs to control a high-performance, multi-stage converter that improves input current quality, reduces harmonic distortion, and ensures high power factor. The additional PWM signals can ensure optimal power flow even under varying load conditions.

3. Simulation and Experimental Results

3.1. Simulation results

Ensuring the functional integrity of the inverter system requires precise configuration of the driving ePWM module. Key operational parameters—such as those defining the switching frequency (via the triangular carrier generation) and the instantaneous duty cycle (derived from comparing the reference sine wave against the carrier)—are programmed into the ePWM's control registers. These register values dictate the behavior of the internal timer/counter logic responsible for waveform generation. Furthermore, a dedicated enabled signal gates the PWM output drivers, controlling the activation of control signals to the inverter power stage. Table 1 enumerates the specific parameter values employed consistently throughout simulation validation and experimental testing.

Table 1. *Parameters used in simulation and experimental*

Parameters	***Value***
Input clock carrier	300MHz
Input clock reference	150MHz
Reference Frequency setpoint	50Hz
Carrier frequency setpoint	15Khz
Timing constraint	100MHz
Synthesis mode	Performance Optimize
WNS (Worst Negative Slack)	-1.28ns
TNS (Total Negative Slack)	-14.72ns

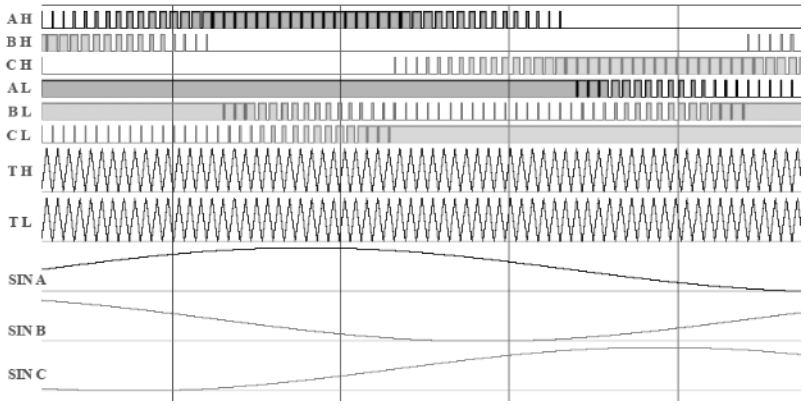

Figure 9. *Vivado Simulation results of control signal waveforms.*

As illustrated in Figure 9, simulation results confirm that the ePWM architecture deployed on the programmable logic (PL) of the XCZU3EG device performs in full accordance with the design specifications. Signal named AH is combination of Signal A, B, C are 3 phase control output, L is control

for modulation output from 0 to V/2 and H is control for modulation output from V/2 to V. TH and TL are carrier waveform and SIN A, B, C are output from reference signal generators. The bidirectional counter block accurately generates a triangular carrier waveform by incrementing and decrementing as required. Carrier signals for each inverter level are synthesized in strict compliance with predefined modulation criteria, with setting values displayed precisely. Additionally, the sine wave generator reliably outputs three reference signals with accurate phase displacement and amplitude. The PWM module then compares these reference signals with their corresponding carriers, producing synchronized and accurate high-side and low-side gate signals for effective inverter control.

To evaluate the actual number of ePWMs achievable and to determine the controller's setting parameters, it is essential to incorporate communication blocks and segment the data stream. Furthermore, the ARM Cortex 53 or Cortex R5 processor block is integral for managing complex tasks. The operation of the system's operating system facilitates the adjustment of controller parameter settings. The comprehensive block diagram of the system is depicted in Figure 10.

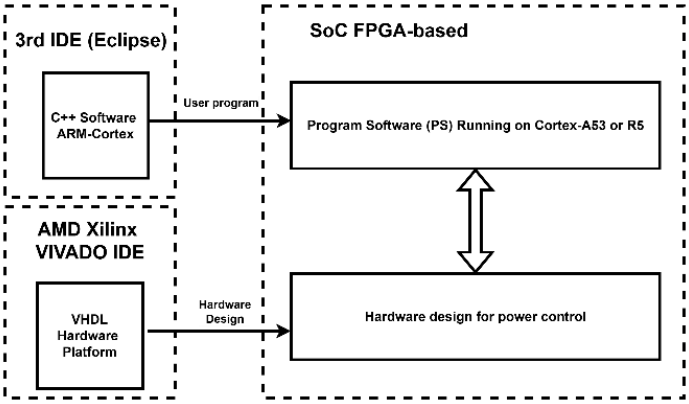

Figure 10. *System programing flow for SoC.*

Figure 10 presents the block diagram of the program for the FPGA-based System on Chip (SoC). The user software is compatible with any ARM compiler. The pre-designed hardware is configured for the FPGA, and the power control peripherals are accompanied by a library that defines the registers. The system resources utilized to construct the system with ten units of a three-level inverter are detailed in Table 2.

Table 2. *Resource used for system design XCZU3EG*

Resource	***Utilization***	***Available***	***Used %***
LUT	9715	70560	13.76
LUTRAM	120	28800	0.42
FF	7272	141120	5.12
BRAM	14.3	216	6.62
DSP	60	360	16.67
IO	121	252	48.01
BUFG	3	196	1.53
PLL	1	5	20.00

Table 2 demonstrates that the new system consumes very few resources. Tasks such as real-time signal processing, AI inference acceleration, or complex cryptographic algorithms can be offloaded to the FPGA for hardware-level speed. This allows for ultra-low-latency performance in applications like radar systems, high-frequency trading, and autonomous vehicles. With high-speed interfaces and five programmable PLLs, it ensures precise timing and high data throughput. The chip’s ability to parallelize

heavy mathematical operations makes it ideal for edge computing, scientific modeling, and other high-performance embedded tasks.

3.2. Experimental results

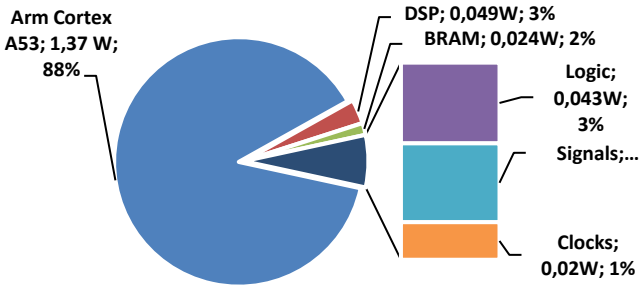

Figure 11. *Power consumption of SoC.*

Analysis of the system power profile, presented in Figure 11, indicates that the Processing System (PS), encompassing the ARM core complex, constitutes the dominant power consumer, accounting for approximately 88% of the total budget. In contrast, resources within the Programmable Logic (PL) fabric—specifically logic elements (LUTs/FFs), Block RAMs (BRAMs), DSP slices, and associated clocking infrastructure—contribute only a minor fraction of the overall power draw. This power distribution is typical for heterogeneous SoC architectures where the high-performance PS handles OS-level tasks and sequential code execution, while the PL implements application-specific accelerators or interfaces. In this specific application, the computational load appears heavily biased towards the PS, resulting in its disproportionately high-power consumption relative to the PL. The inverter's operation is controlled by three registers that specify the PWM settings, the triangular carrier wave, and the sinusoidal reference wave. The memory map for Inverters 1 and 2 (of 10 total) is detailed in Figure 12.

	32 bit Register	Memory Addr
No1	PWM Config Register	0x43C00000
	Sawtooth Config Register	0x43C00004
	Sine Config Register	0x43C00008
No2	PWM Config Register	0x43C00012
	Sawtooth Config Register	0x43C00016
	Sine Config Register	0x43C00020

Figure 12. *Hardware physical address and register configuration.*

Figure 13. *Output signal capture from DSO.*

The Logic Analyzer DSlogic Plus 400MHz was used to capture the switch signal from the experimental setup. Figure 13 illustrates the control signal for the 12 switch devices of the three-level inverter.

Featuring a total of 10 units with outputs akin to those shown in Figure 13. This demonstrates that the SoC can manage 10 three-phase, three-level inverters simultaneously. Additionally, the SoC retains 56 IO resources for other functions such as ADC, Interrupt, communication, and more.

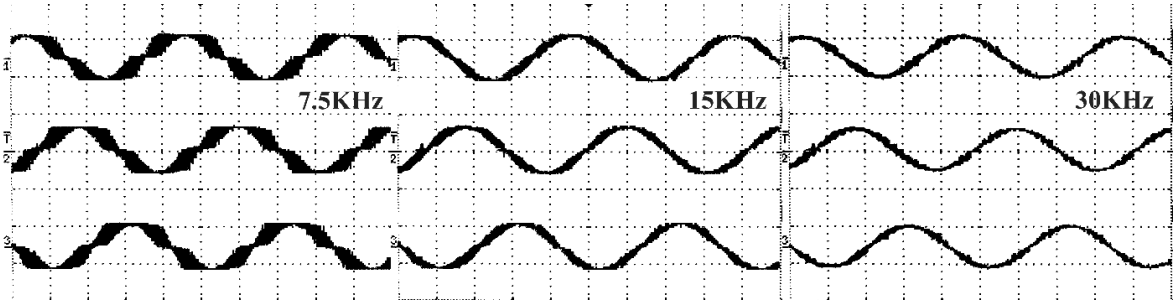

Figure 14. *Voltage output 3L inverter at Fs 7.5Khz, 15Khz and 30Khz.*

Figure 14 demonstrates that the output waveform at 7.5 kHz distinctly exhibits all three voltage levels: V+, V-, and 0. This observation substantiates that the design model and algorithm operate correctly in accordance with the specified requirements. The results show the influence of switching frequency on the output quality. However, at the cost of switching loss, with GaN/SiC components, switching loss at high frequencies can be significantly reduced.

4. Conclusions

Addressing the increasingly critical need for high-density, precisely synchronized PWM signal generation, particularly in complex multi-level inverter control systems, this paper details a comprehensive FPGA-based System-on-Chip (SoC) control architecture. The proposed solution strategically exploits the unique advantages of FPGA technology, particularly its fine-grained reconfigurability and inherently parallel structure, allowing for the design of highly customized I/O interfaces and parallel data paths. This enables the concurrent management of potentially hundreds of precisely timed PWM channels, effectively circumventing the fixed peripheral limitations and sequential processing bottlenecks commonly encountered with traditional DSP controllers when attempting to scale control complexity and output density.

Key architectural features developed within this framework include the instantiation of multiple high-resolution ePWM modules, designed with configurable dead-band insertion for shoot-through prevention and exceptional timing precision vital for minimizing switching losses and harmonic distortion. A distinctive aspect of the design is the integrated control logic for an auxiliary buck/buck-boost power stage, which incorporates dedicated ADC-based Maximum Power Point Tracking (MPPT) functionality. This embedded power stage allows for efficient on-board power management and regulation, potentially enabling self-powered system operation or facilitating a direct, optimized interface with variable renewable energy sources like photovoltaic arrays.

Ultimately, this work delivers a highly adaptable hardware platform capable of implementing advanced, high-performance closed-loop control strategies. Its capabilities span diverse applications, including sophisticated power quality management and precision motion control. The platform's modular design and scalability make it exceptionally useful. It serves as a vital tool for academic researchers exploring novel control techniques and for industry professionals needing to rapidly prototype or deploy next-generation modular power converters. This platform can also accelerate development and validation, partly through its integrated support for hardware-in-the-loop (HIL) testing.

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