A REVIEW PAPER ON RADIAL JUNCTION SILICON NANOWIRE SOLAR CELLS

BÀI BÁO TỔNG HỢP VỀ CÁC THIẾT BỊ PIN NĂNG LƯỢNG MẶT TRỜI ĐƯỢC LÀM TỪ DÂY NANO SILICON TRÊN CƠ SỞ CẤU TRÚC TIẾP GIÁP XUYÊN TÂM

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ABSTRACT

In recent years, demand of using energy, especially renewable energy is increasing rapidly in worldwide. The traditional energy sources based on coal, oil… are not friendly with environment and the verge of ending. Another energy source is nuclear energy, however it is restricted to spread out because of risk of radioactive leakage although it stores a huge potential to support enough energy for mankind in the future. In this situation, solar energy is becoming the brightest alternative energy source for the mankind. Many different solar cell structures based on different materials have been studying follow to the target of high-performance and cost effective solar cells. Among solar cell structures, silicon nanowire solar cells based on radial junction structure are attracting the attention because of its unique properties such as reduced reflection, extreme light trapping, increased defect tolerance, reduced material amount... This paper will review recent developments in this structure, includes silicon nanowire synthesis, radial junction solar cells fabrication, challenges to obtain low cost and high-performance silicon nanowire solar cells.

Keywords: *Nanowire solar cells; Silicon nanowires; Radial junction solar cells; Renewable energy; Nanowires synthesis*

TÓM TẮT

Những năm gần đây nhu cầu sử dụng năng lượng, đặc biệt là năng lượng sạch có thể tái tạo được đang tăng nhanh chóng trên toàn thế giới. Các nguồn năng lượng truyền thống hiện nay trên cơ sở than đá, dầu… không thân thiện với môi trường và hầu như đang trên bờ vực cạn kiệt. Một trong những nguồn năng lượng khác là năng lượng hạt nhân, tuy nhiên nó bị hạn chế để mở rộng bởi các nguy cơ rò rỉ phóng xạ mặc dù tích trữ một tiềm năng to lớn để cung cấp đủ năng lượng cho nhân loại trong tương lai. Trong tình hình này, năng lượng mặt trời trở thành nguồn năng lượng thay thế sáng giá nhất cho nhân loại. Nhiều cấu trúc pin năng lượng mặt trời trên cơ sở các vật liệu khác nhau đã được nghiên cứu theo hướng hiệu suất cao, giá thành thấp. Trong số các cấu trúc pin năng lượng mặt trời, cấu trúc pin năng lượng mặt trời trên cở dây nano silicon dạng tiếp giáp xuyên tâm đang cuốn hút sự quan tâm lớn bởi các đặc tính đặc biệt của nó cho ứng dụng làm pin năng lượng mặt trời như giảm sự phản xạ ánh sáng, tăng bẩy sáng, khả năng chịu đựng sai hỏng cao, không cần sử dụng nhiều vật liệu… Trong bài báo này chúng tôi sẽ tổng hợp lại những sự phát triển gần đây của pin năng lượng mặt trời được làm từ dây nano silicon trên cơ sở cấu trúc này, bao gồm quá trình tổng hợp dây nano silicon, quy trình chế tạo cấu trúc pin năng lượng mặt trời dạng kết nối xuyên tâm, thảo luận các thách thức để tạo ra các cấu trúc pin năng lượng mặt trời trên cơ sở dây nano silicon có hiệu suất cao và giá thành thấp.

Từ khóa: *Pin năng lượng mặt trời trên cơ sở dây nano; Dây nano silicon; Pin năng lượng mặt trời cấu trúc xuyên tâm; Năng lượng tái tạo, Sự tổng hợp dây nano.*

1. INTRODUCTION

Demand for energy is increasing day by day, meanwhile natural fossil fuel sources are becoming less and less available; moreover, burning fossil fuels is not responsible, since it can lead to uncontrollable climate change in the future. So there is high necessity for alternative renewable energy sources for the coming decades. Among various energy sources including hydroelectricity, biomass, wind, and geothermal energy, sunlight is the most abundant natural energy resource. While the energy from sunlight striking the earth in one hour can meet our annual global energy consumption, however most of the sunlight energy is lost. In principle, photovoltaics (PV), or the direct generation of electric power from sunlight, might be able to provide enough energy to support the increasing energy demand of mankind [1].

In the past decades, great efforts have been undertaken to develop various inorganic and organic PV devices [2]. The single-crystalline Si solar cell, invented 50 years ago [2], remains the basis of the current PV industry due to the abundance of Si materials and the high reliability and relatively high efficiency of Si PV. However, the high cost of Si PV, due mainly to the high cost of solar-grade Si wafers as well as encapsulant, has restricted the mass deployment of Si PV. To reduce the cost, extensive efforts have focused on the development of less expensive thin-film solar cells [3], such as amorphous Si (a-Si), polycrystalline Si (pc-Si), cadmium telluride (CdTe), copper indium gallium selenide (CIGS), and polymer-based PV. While these PVs have achieved high enough efficiency for practical usage, they are still not cost-competitive against traditional fossil fuels. Consequently, great efforts have been directed to develop new designs for solar cells via unconventional approaches, aiming at cost reduction and performance improvement [4]. In this quest, a number of new strategies that may substantially improve the performance and lower the cost of PV have emerged. Of particular interest is the PV designs based on nanostructured materials, such as nanocrystals (or quantum dots, nanoparticles) [5], nanotubes [6], nanorods (or nanopillars) [7], and nanowires [8], which provide unique advantages in terms of strong light absorption and efficient charge separation owing to their large surface areas. In particular, one-dimensional (1D) semiconductor nanowires, with direct wire paths for charge transport and high surface area for light harvesting, are emerging as a promising candidate for building PV devices. Among 1D nanostructures, Si nanowires (SiNWs) are widely considered as an important material for high-performance devices [9] due to their unique structural, electrical, optical, and thermoelectric properties. Presently, SiNWs are under intense investigation for PV applications since they can create novel solar-to-electric energy conversion approaches for both high device efficiency and simple, low-cost manufacturing [10]. Solar cells based on NWs can mainly have three geometries as shown in figure 1 [11] include radial, axial and substrate junction. Every structure has individual its advantages and drawbacks. For radial junctions (Figure 1a), this structure has many advantages compared with axial junction (Figure 1b) and substrate junction (Figure 1c) such as high light trapping (periodic array of SiNWs), low recombination (charge separation along the NWs' radius), high defect tolerance and is promising to produce low-cost solar cells in the third solar cell generation. In this work, we will focus on silicon nanowire radial junction solar cell structures, which were fabricated successfully, discussing advantages, drawbacks, spaces for improving more the structure, the target is led to high efficiency, low-cost solar cells for PV market in the future.

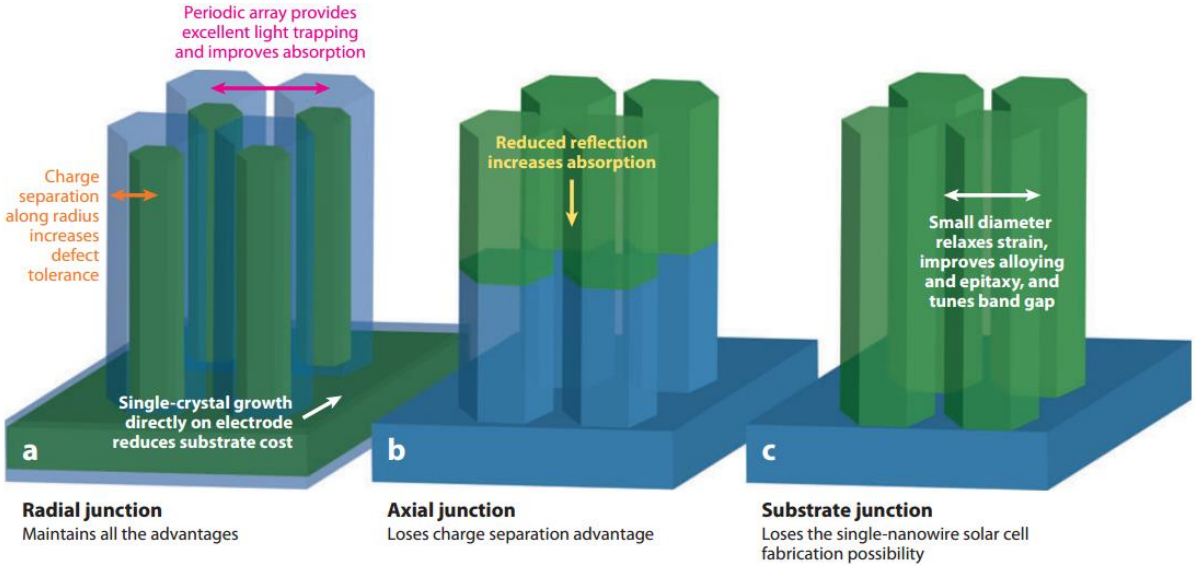

Figure 1. *Various nanowire solar cell geometries. (a) Periodic arrays of radial junctions combine several advantages, such as extreme light trapping, radial charge separation, relaxed interfacial strain, or single-crystalline growth on non-epitaxial substrates. (b) In axial junctions, the benefit of radial charge separation is lost. (c) Substrate junctions lack the radial charge separation benefit and cannot be removed from the substrate to be tested as single-nanowire solar cells. Figure is reused from the Ref [11].*

2. SYNTHESIS OF SILICON NANOWIRES FOR RADIAL JUNCTION SOLAR CELLS

Silicon nanowires for radial junction solar cells can be prepared based on bottom-up or top-down fabrication.

2.1. Bottom-up fabrication

Bottom-up fabrication is a growth process which joining Si atoms to form SiNWs. This approach includes many different techniques such as vapor-liquid-solid (VLS) or vapor-solid-solid (VSS) based on chemical vapor deposition (CVD) system, oxide – assisted growth (OAG), molecular beam epitaxy (MBE), laser ablation… However, among these methods, vapor-liquid-solid (VLS) or vapor-solid-solid (VSS) based on chemical vapor deposition (CVD) system (figure 2) is the most common method and it is widely used. Both of two mechanisms use metal catalyst such as gold (Au), aluminum (Al), copper (Cu)… for growth. This section will focus on these two growth mechanisms.

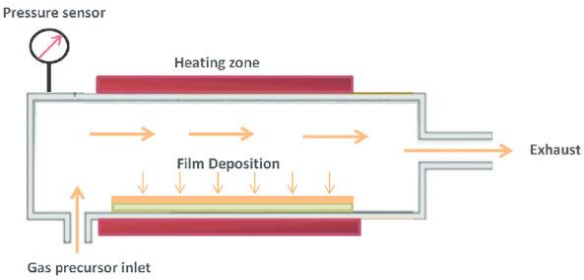

Figure 2. *Schematic diagram of a chemical vapor deposition (CVD) system. Figure is reused from the Ref [12]*

Concerning the VLS mechanism, the growth temperature must be equal or higher than the eutectic temperature point of the metal-semiconductor alloy, in order to form liquid droplets. This mechanism is illustrated on figure 3, a gaseous precursor (for instance SiH_4 or $SiCl_4$) decomposes as it reaches the metal catalyst's surface, the liquid metal/semiconductor alloy will absorb Si atoms until it reaches saturation. Then Si atoms precipitate at the liquid – solid (substrate) interface leading to the growth of c-SiNWs.

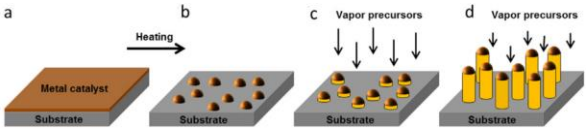

Figure 3. *Schematic illustration of the VLS process. (a) A metal catalyst layer is deposited on the substrate. (b) Upon heating, dewetting of the metal layer forms small droplets. (c) Introduction of vapour precursors leads to incorporation of the precursor inside the droplet and its precipitation at the catalyst–substrate interface. (d) Growth of c-SiNW. Figure is adapted from Ref [13]*

Concerning the VSS mechanism, the growth temperature is lower than the eutectic temperature point. SiNWs will grow from solid particles of a metal catalyst. Si atoms are absorbed in the metal catalyst until the solid alloy particles reach saturation. Then Si atoms precipitate at the solid – solid (substrate) interface (between the alloy and the substrate) leading to the growth of c-SiNWs.

Compared to VLS, VSS has two advantages: a lower growth temperature and a lower solubility of Si in the alloy (about one order of magnitude), it means VSS uses less material for growth than VLS. However, the VSS's growth rate is very slow (~ tens of nanometer/minute). Figure 4 shows SEM images of SiNWs grown from various catalysts following a VLS or a VSS mechanism.

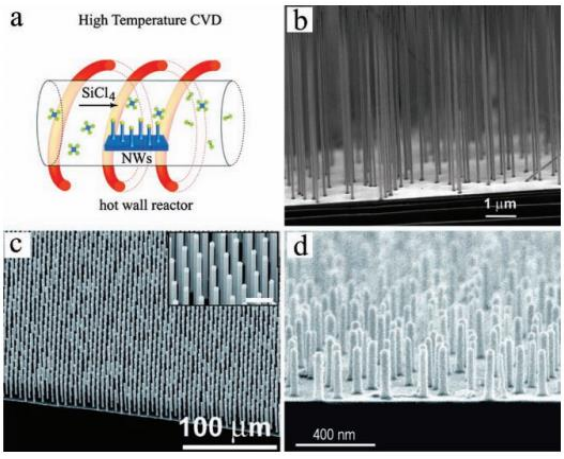

Figure 4. *a) Schematic of a high-temperature hot wall CVD setup. b) Scanning electron microscopy (SEM) cross-sectional image of a SiNWs array grown by VLS from Au colloids. c) Tilted SEM view of a Cu-catalyzed Si wire array grown by VLS-CVD over a large (>1cm^2) area. The scale bar in the inset is 10 μm. d) SEM cross-sectional image of Al-catalyzed SiNWs array on Si(111) grown at 430°C by VSS. Figure is reused from Ref [14].*

Gold (Au) is the most common metal catalyst used for bottom-up growth of Si nanowires because the Au – Si eutectic temperature point is quite low (~ 363^0C)[15] as seen in figure 5, but the remain gold contamination of the SiNWs creates traps at mid-gap of silicon as shown at the figure 6, which are very effective recombinations centers. Those traps capture electrons and holes making as-grown NWs unsuitable for electronic applications, and even worse for PV applications. Moreover, with most of the metal catalyst (Au, Cu, …), one needs to add a potentially harmful dopant precursor (PH_3 and B_2H_6) during the CVD process to dope the SiNWs. Consequently, alternative CMOS (complementary metal-oxide-semiconductor)-friendly metals such as aluminum (Al), gallium (Ga) or indium (In) are used, those contaminants, which are also p-type dopants (column III of the table of the elements) introduce energy levels situated far from the silicon's midgap [16] (figure 6).

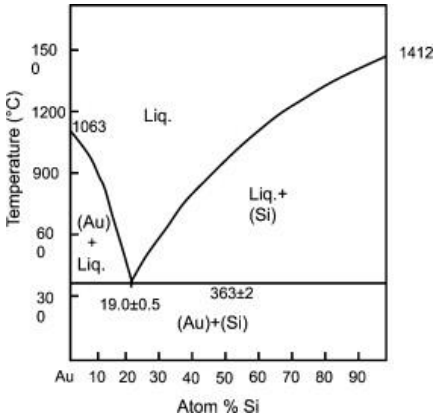

Figure 5. *Au-Si phase diagram. Figure is reused from Ref [15]*

One of friendly metal catalysts are chosen for SiNWs growth in electronic field is aluminum (Al), since Al contaminants induce shallow energy level in the bandgap (figure 6), besides the resulting SiNWs will be p-doped without adding any doping gas to the process.

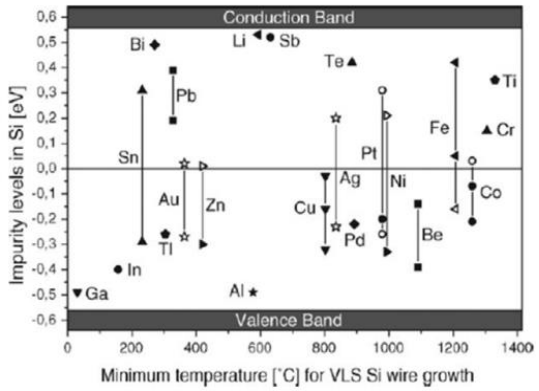

Figure 6. *Energy levels for different impurities in Si with respect to the middle of the band gap and as a function of the minimum temperature required for VLS growth. The lines connect the defect energies available for the same impurity. Figure is adapted from Ref [*16*].*

2.2. Top-down fabrication

In contrast with bottom-up fabrication, top-down approach will reduce the size of Si bulk until it reaches the size of nanowires based on etching technique. This approach has two main techniques to obtain SiNWs: Reactive ion etching (RIE) and Metal-catalyzed electroless etching of silicon (MCEE).

2.2.1. Reactive ion etching (RIE)

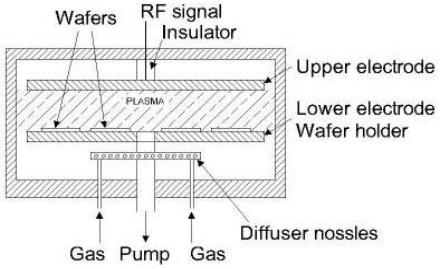

Figure 7. *Structure of reactive ion etching system. Figure is reused from website: [https://www.memsnet.org/about/processes/etch.html]*

Large areas of highly uniform SiNWs can readily be fabricated on Si wafers by this method. Lithography techniques such as photolithography, nanosphere lithography, or nano-imprint lithography… can be used to design a mask for further reactive ion etching in this SiNWs fabrication process. In a RIE system (figure 7), a RF power source turns a gas mixture into a plasma. The ions are accelerated towards the surface and react both physically (depending on the power) and chemically (depending on the gas) with the Si wafers' surface to etch and form SiNWs structure. With RIE, arrays of <100> oriented SiNWs with a controlled size, density and electronic properties can be obtained easily. For instance Hsu *et al*. fabricated uniform Si nanopillars over an entire 4 inch wafer by combining Langmuir–Blodgett assembly and RIE [17] (figure 8).

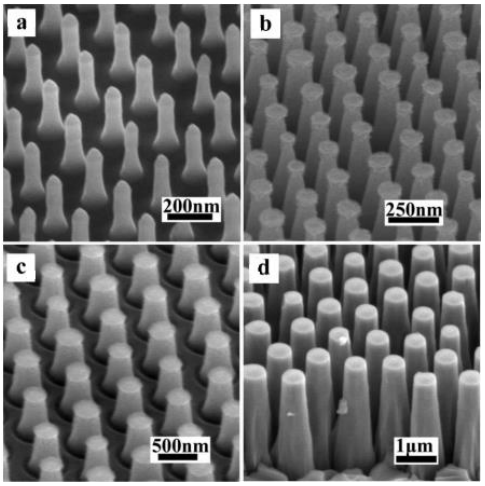

Figure 8. *SEM images of nanopillars arrays with uniform tip diameters of a) 60, b) 125, c) 300, and d) 600 nm were obtained by Reactive Ion Etching. Figure is adapted from Ref [17].*

2.2.2. Metal-catalyzed electroless etching of silicon (MCEE)

In 2002, Peng *et al*. [18] reported that a wafer-scale SiNWs array could be readily produced via electroless etching at room temperature by simply dipping Si wafers into a HF–$AgNO_3$ solution. Highly oriented SiNWs arrays and Si nanostructures including porous Si and Si nanoholes can be obtained by metal-catalyzed (commonly silver or gold) electroless etching (MCEE) of Si wafers in a HF solution containing oxidizing agents, such as $Fe(NO_3)_3$ or $AgNO_3$. They proposed a microscopic mechanism for the MCEE method based on metal-induced local oxidation and anisotropic dissolution of oxide in the HF-containing solution. Beginning of this SiNWs fabrication process is to deposit metal particles such as Ag, Ni, Au, Fe… on Si

wafer's surface (after removing totally SiO_2 film on them), these metal particles will attract electrons from Si zone where they touch, this will lead to oxidation of that Si zone (figure 9a). By this way, when those Si wafers were dipped in HF solution, the oxide Si zone will be etched by HF, this process will repeat many times until nanowire structure is formed (figure 9b). The metal movement was preferentially along the Si [100] crystallographic orientation, thus leading to anisotropic Si(100) etching (figure 10).

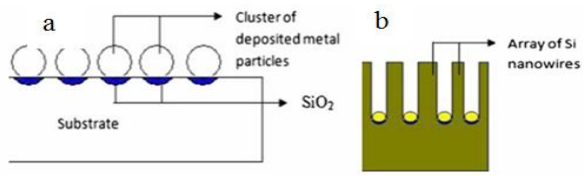

Figure 9. *(a) Oxidation of silicon surface under deposited metal, (b) Formation of silicon nanowires by electroless metal deposition. Figure is adapted from Ref [19]*

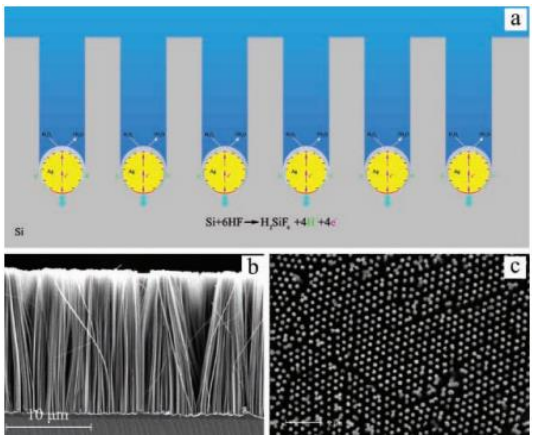

Figure 10. *a) Schematics of collective and extended tunneling motion of Ag (or other metal) particles in a Si matrix leading to the formation of Si nanostructures. b) Cross sectional SEM image of aligned SiNWs arrays obtained by Ag-catalyzed electroless etching of p-type Si(100) in aqueous HF/H_2O_2 solution. c) SEM image of ordered arrays of SiNWs with controlled diameter and density by combination of MCEE and nanosphere lithography techniques. Figure is reused from Ref [14].*

Between the top-down and bottom-up fabrication process, MCEE is simple and does not require any expensive equipment. Moreover, it is a low-temperature and scalable method. However, a severe drawback of this method is that it relies on the use of monocrystalline (or at least multicrystalline) Si substrates which are very expensive.

3. PROPERTIES OF SILICON NANOWIRES FOR PHOTOVOLTAIC APPLICATIONS

3.1. Electronic properties of silicon nanowires

The electronic properties of SiNWs have been studied by numerous theoretical and experimental investigations. SiNWs are prepared via the "top-down" and "bottom-up" method have different electrical properties. In the top-down process (RIE etching or MCEE), SiNWs inherit the electrical characteristics of the mother Si wafers and do not need further doping. In contrast, SiNWs produced via the bottom-up method are generally intrinsic and need to be doped for future use in different electronic applications. Dopant can be incorporated during growth by adding precursors such as diborane and phosphine for p- and n-type doping respectively or by ion implantation. In 2000, Y. Cui *et al*. reported about the fabricating of n- and p-type SiNWs by introducing boron or phosphorus dopants, during SiNWs growth [20]. The doping level and mobility of the SiNWs was indicated directly via FET (Field Effect Transistor) devices. The performance of a device depends strongly on carrier mobility, so efforts have focused on improving the carrier mobility in SiNWs. The surface properties of SiNWs are expected to have a strong influence on the electrical characteristics owing to their large surface-to-volume ratios. Cui *et al* reported remarkably enhanced carrier mobility in SiNWs after thermal annealing and chemical surface passivation via chemical modifications. An average mobility of 30–560 $cm^2V^{-1}s^{-1}$ with a peak value of $1350cm^2V^{-1}s^{-1}$ [21] was achieved after surface treatment of SiNWs p-type (Boron-doped). It is however very likely that the value of 1350 $cm^2V^{-1}s^{-1}$ is due to a wrong measurement, since it has never been

reproduced; moreover, we cannot understand how a p-type Si sample could have such a high mobility, about 3 times larger than any high quality p-doped monocrystalline sample.

Besides, in the bottom-up process, as mentioned conducting SiNWs can also be directly grown by using the metal as a dopant without the need of a precursor. For example using aluminum as a catalyst (a column III element) directly results in p-doped SiNWs [22]. Another advantage is that the dopant profile (*i.e.*, Al itself in this case) is uniform along the radial and axial directions of the Si wire [23].

3.2. Optical properties of silicon nanowires arrays

SiNWs arrays can increase light trapping and thus optical absorption leading to highly efficient solar cells. SiNWs have diameters usually smaller than the visible light wavelengths and act as an antireflection subwavelength structure [24]. Light reflection can be further reduced with tapered SiNWs because the refractive index changes gradually with NWs diameter from the air down to the roots of SiNWs.

Peng *et al.* reported that SiNWs arrays prepared by the MCEE method exhibit excellent antireflection properties [25–28]. Figure 11a shows the reflectance of MCEE-SiNW arrays on single-crystal and polycrystalline Si wafers, porous Si, and polished single-crystal Si wafers. It clearly shows that SiNWs arrays have low light reflectance over a wide spectral bandwidth. Low light reflection has also been obtained with bottom-up SiNWs: Tsakalakos *et al*. have shown in 2007 that SiNWs grown by CVD on stainless steel can have a significantly reduced reflectance (<1%) (Figure 11b) [29].

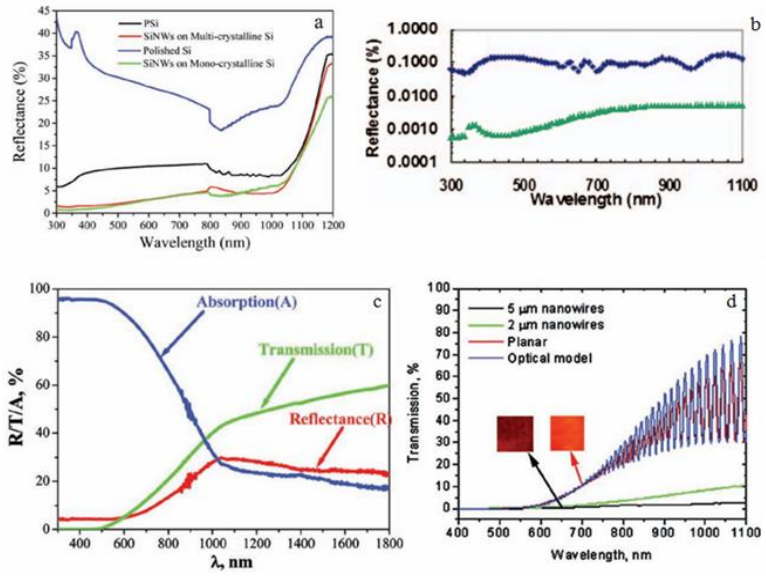

Figure 11. *a) Reflectance measurements of SiNW arrays, porous Si (PSi), and polished crystalline Si. The PSi was prepared by conventional etching in a HF/HNO_3 solution. Figure is reused from the Ref [14].b) Reflectance measurements of SiNW arrays (green) grown by CVD compared to a thin film p-i-n a-Si solar cell (blue). Figure is adapted from the Ref [29]. c) Optical transmission (T), reflectance (R), and absorption (A =1–T–R) of SiNWs prepared by etching of 2.7- μm-thick mc-p^+nn^+-Si layers on glass. Figure is adapted from the Ref [30] d) Transmission spectra of thin Si window structures before (red) and after etching to form 2 μm (green) and 5 μm (black) nanowires. The spectrum from an optical model for a 7.5- μm-thin Si window is in blue and matches very well with the planar control measurement. The insets are backlit color images of the membranes before and after etching. Here there is a large intensity reduction and red shift in the transmitted light after nanowires formation, suggesting strong light trapping. Figure is reused from the Ref* [24].

Besides, SiNWs arrays increase light absorption because the photons can be scattered several times between the SiNWs then increase the probability for photons to be absorbed. Figure 11c shows that SiNWs films have a very low reflectance (<10% at 300–800 nm), a strong broadband optical absorption (> 90% at 500 nm), which is much higher than Si films of the equivalent thickness. Optical transmission and photocurrent measurements (figure 11d) have shown that the transmission of incident solar radiation (AM 1.5G) in SiNWs array can be increased by 73 times compared to a flat surface [24].

4. FABRICATION OF RADIAL JUNCTION SILICON NANOWIRE SOLAR CELLS

As mentioned, in the three main nanowire solar cell structures the radial junction nanowire solar cell structure has many advantages which are propitious for converting light photons into electricity with the least carriers loss. This structure can be designed on inexpensive substrates (stainless steel, aluminum, glass…), this is basis for low cost solar cells. This section will review the published solar cells, strong and weak points of this structure, discussing about issues for improving to reach high-performance and cost-efficient solar cells.

4.1. Single radial p-n junction

In 2007, Tian *et al.* reported a structure of a single p-type/intrinsic/n-type (p-i-n) coaxial (or core-shell) SiNW solar cell. The p-type SiNW core was prepared by gold-catalyzed VLS growth, using SiH_4 as the Si precursor and diborane (B_2H_6) as the p-type dopant. Then, Si i- and n-shells (PH_3 doping) were deposited sequentially outside p-type core [31]. Figure 12a illustrates the fabrication process of the p-i-n coaxial SiNW solar cell and the corresponding SEM images are shown in figure 12b. Under AM 1.5G illumination (AM 1.5G is standard spectrum at the Earth's surface, its power density around 970W/m^2, in reality it has been normalized to give 1kW/m^2 for solar simulation in solar cell testing), the p-i-n coaxial SiNW solar cell yielded a maximum power output of 200 pW per nanowire device, a large short-circuit current density (J_{sc}) of 23.9 mAcm^{-2} (upper bound), and an overall power conversion efficiency of 3.4% (upper bound). J_{sc} was linearly scalable with wire length while the open-circuit voltage (V_{oc}) was essentially independent of the length. The results indicated that photoexcited carriers were collected uniformly along the length of the radial p-n junction structures and that light scattering by metal contacts did not make a significant contribution to the observed photocurrent. This is the first structure of a single radial p-n junction was obtained based on silicon nanowires and it really demonstrated the potential of SiNWs for photovoltage application and create stable background for later structures.

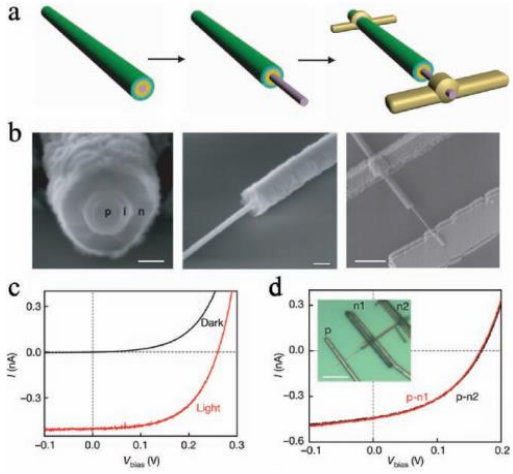

Figure 12. *Fabrication and characterization of the p-i-n silicon nanowire photovoltaic device. a) Schematics of the device fabrication. Left: pink, yellow, cyan, and green layers correspond to the p-core, i-shell, n-shell, and PECVD-coated SiO_2, respectively. Middle: selective etching to expose the p-core. Right: metal contacts deposited on the p-core and n-shell. b) SEM images corresponding to the schematics in (a). Scale bars are 100 nm (left), 200 nm (middle), and 1.5 mm (right). c) Dark and light current–voltage (I–V) curves. d) Light I–V curves for two different n-shell contact locations. Inset is an optical microscopy image of the device. Scale bar is 5 mm. Figure is adapted from Ref [31].*

4.2. Radial junction silicon nanowire arrays were grown on substrate

Among solar cells structures based on SiNWs, radial p-n (p-i-n) junction SiNWs arrays have numerous advantages for efficient light harvesting, owing to their array geometry. First, the geometry of SiNWs arrays possesses strong antireflection characteristics, which helps SiNWs solar cells to absorb nearly all the sunlight with an energy above the Si band gap. Second, the radial p-n junction nanowire geometry offers efficient carrier separation and minimal bulk recombinations, since minority carrier diffusion lengths are usually longer than the diameter of the wires. Hence, the radial geometry enables to lower the Si quality. Third, a few percent of the Si quantity needed for wafer-based solar cells is necessary for wire-based cells. Finally, scalable methods, such as CVD-VLS and MCEE, can be used to prepare vertically aligned SiNWs over large areas on various substrates. These advantages make solar cells based on arrays of SiNW radial p-n junctions highly promising for mass deployment.

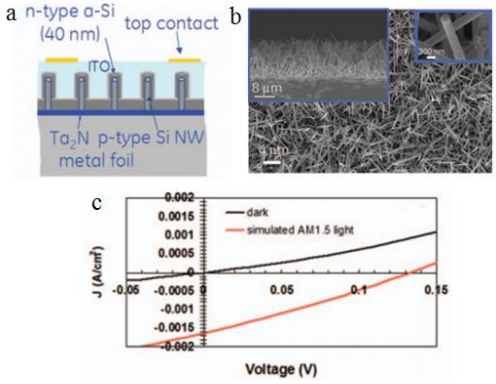

Figure 13. *a) Schematic cross-sectional view of the SiNW solar cell structure. The nanowire array is coated with a conformal α-Si:H thin-film layer. b) SEM image of a typical SiNW solar cell on a stainless steel foil, including a-Si and indium tin oxide (ITO) layers with insets showing a cross-sectional view of the device and a image of an individual SiNWs coated with a-Si and ITO. c) Dark and light (under simulated AM1.5 conditions) I– V characteristics of the cell. Figure is adapted from Ref [29].*

In 2007, Tsakalakos *et al.* [29] have fabricated p-n junctions SiNW-array solar cells by growing p-type SiNWs arrays via CVD-VLS on stainless steel foils, followed by a conformal coating of n-type amorphous Si film via a PECVD process (figure 13). Under AM 1.5G illumination, their best SiNW-based PV device yielded a V_{oc} of 130 mV and a conversion efficiency of 0.1%, this result is by far large small compared to the calculated 15–18% for an ideal SiNW-based solar cells. The authors suggested that the low conversion efficiency may be improved by optimizing the nanowire diameter, improving the radial p-n junction, reducing the contacts resistances, and minimizing shunts [29].

In 2009 Gunawan *et al.* fabricated solar cells from Au catalyzed CVD-VLS grown SiNWs on a Si(100) substrate. Each SiNW of a n-type core, subsequently coated with a layer of highly conducting p-type polycrystalline Si shell to make p-n junction. This structure increased light trapping, but the gold impurities affected the minority carrier lifetime in Si leading to enhanced carrier recombinations. The surface recombinations were effectively mitigated by an ALD-grown Al_2O_3 passivation layer that improved the solar conversion efficiency from 1% to 1.8% [32].

In 2010 Putnam *et al.* introduced VLS-grown Si microwire-array solar cells with 7.9% efficiency (V_{oc} ~ 500mV, FF ~ 65% under AM 1.5G illumination), using a a-SiN_x:H passivation layer [33]. Next Kelzenberg *et al.*, demonstrated that VLS-grown Si microwires can have high-performances for photovoltaic applications (long minority-carrier diffusion lengths (L_n >> 30µm) and low surface recombinations velocities, S << 70cm.s^{-1}) by using amorphous silicon (a-Si) and silicon nitride (a-SiN_x:H) as passivation layers. Their single-wire radial p-n junction cell reached 9% efficiency (V_{oc} ~ 600mV, FF ~ 80%), they also predicted that large-area Si wire-array solar cells can potentially exceed 17% energy-conversion efficiency in the future [34].

Besides CVD-VLS growth, MCEE and RIE SiNWs arrays are promising for radial p-n junction SiNWs arrays solar cells (simple process, low-temperature, readily scalable method…). Figure 14 shows the structure and electrical characteristics of such a solar cell. Single-crystalline MCEE n-SiNWs with diameters from 50–100 nm were coated with a layer of 150nm-thick a-Si p-type (boron doping) shell. This layer then is converted to polycrystalline shell after a rapid thermal processing (RTP) at 1000°C in 10s, the rear and front side contact electrodes were formed by sputtering Ti/Ag onto the n-Si and Ti/Pd onto the p-Si. Under AM 1.5G illumination, the devices gave overall efficiency of about 0.46% [35]. This result was improved by reducing the surface roughness of the SiNWs and by adjusting the nanowires diameters and density, leading to an improved conversion efficiency (5–6%) [24], despite the high interfacial recombination because of the high surface area of the SiNWs.

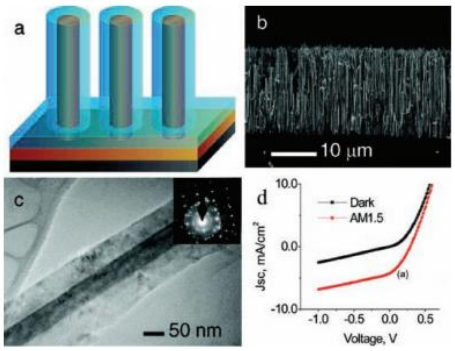

Figure 14. *SiNWs solar cell structure. a) Schematic cell design with the single crystalline n-SiNW core in brown, the polycrystalline p-Si shell in blue, back contacts are in black. b) Cross-sectional SEM image of a completed device demonstrating excellent vertical alignment and dense wire packing. c) Transmission electron microscopy (TEM) image showing the single crystalline n-Si core and polycrystalline p-Si shell. The inset is the selected area electron diffraction pattern. d) Current-voltage behavior in the dark and under AM1.5 simulated sunlight irradiation. Figure is adapted from Ref [35].*

In the recent years, many efforts have focused on improving the efficiency of this kind of structure, leading to significant results. As mentioned above, Kelzenberg *et al*. obtained 9% efficiency by improving the surface passivation on a single-wire cell [33,34]. In 2013 Misra *et al*. optimized the density of the SiNWs via a plasma-assisted vapor–liquid–solid process on glass substrates. They achieved a radial hereojunction c-Si/a-Si:H solar cell structure (Figure 15a) with an open circuit voltage of 0.80V, a short circuit current density of 16.1 mA/cm^2 and a high power conversion efficiency of 8.14% [36]. Furthermore, they showed experimental evidence of the excellent stability of such a radial heterojunction c-Si/a-Si:H solar cells with a light-induced degradation of only ~ 6%, compared to the typical degradations of 15% to 20% in planar cells (Figure 15b). Those results indicate the feasibility of such an approach and paves the way towards a new generation of stable and high performance c-Si/a-Si:H thin film solar cells. In 2015, Misra *et al*.[37] keep announcing many improvements on this structure, for instance by modifying the SiNW/a-Si:H interface (adding a very thin p-type a-Si ~ 10nm with a gradien doping level on p-SiNWs before intrinsic a-Si:H coating), the V_{oc} reached ~ 0.9V, by increasing the band gap of the window layer will raise the absorption of blue light and by changing the active material to c-Si will broaden the absorption to near infrared spectral regeion. In their experiment, by replacing n-type a-Si:H by n-type µc-SiO_x:H for window layer, the current density was improved to 15.2mA/cm^2 and lead an overall efficiency of 9.2% [37]. These results will be an important basis for building high performance tandem solar cells based on silicon nanowires.

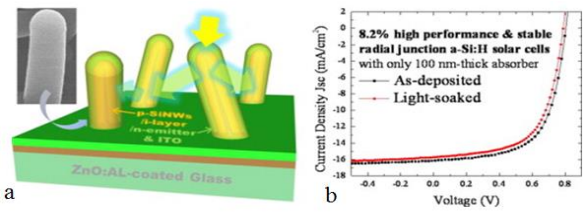

Figure 15. *(a) Schematic illustration of radial junctions solar cells built on top of*

randomly oriented crystalline Si nanowires by subsequent deposition of intrinsic a-Si:H, n-type a-Si:H layers, and a transparent ITO contact, (b) J–V characteristics, as-deposited (black) and after 120 h (red) of light soaking, for the best device. Figure is adapted from Ref [36].

One of issues which reduces the efficiency of nanowire solar cells is top contact's quality, in almost cases ITO film is usually chosen for the top contact, however ITO film is coated surround SiNWs has never been uniform because of shadow phenomenon between SiNWs, resulting series resistance of the cell will be high, consequently the efficiency will be low, moreover it is difficult to make passivation for SiNWs's surface to restrict surface recombination when ITO film is used as top contact in silicon nanowire solar cells. In 2015, Le Duc Toan *et al*. introduced a novel technique for top contact in nanowire solar cells without any transparent conducting material, they used metal $NiSi_x$NWs randomly contact with radial p-i-n SiNWs as shown in figure 16. These metal $NiSi_x$NWs work as top contact for collecting electrons. The best cell has reached the fill factor (FF) value of ~ 74%, this value is the highest FF value for nanowire solar cells so far and the efficiency of the cell is ~ 4.4% with only 33% area of the footprint of the device was covered with p-i-n SiNWs [38]. This result has opened ways for improving the top contact in SiNW solar cells.

Another important issue is that the preparation of SiNW solar cells in modules for real application. This issue was solved for first time by Mutaz Al-Ghzaiwat *et al*. in 2018, they demonstrated a large area ($5x5cm^2$) radial junction silicon nanowire solar mini-modules based on laser scribing technique [39] has operated and yielded a efficiency of ~ 1.32% (6 cells in a module). This efficiency is quite low, but it is a very important first step for applying radial junction silicon nanowire solar cells in reality life in next time.

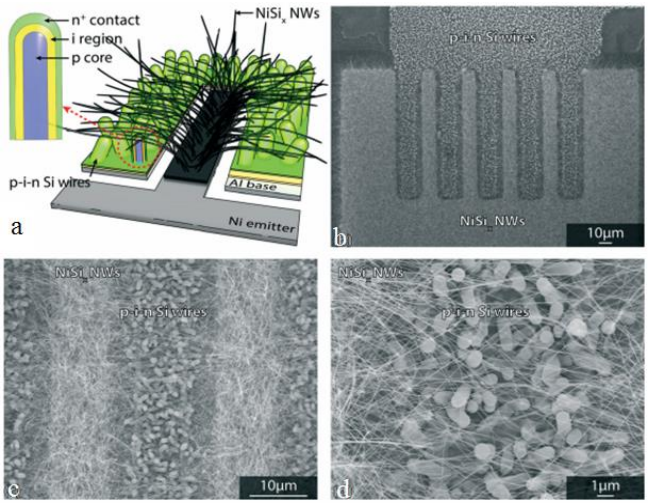

Figure 16. *The interdigitated solar cell structure. (a) Schematics showing a perspective view of two Al fingers (base contacts) supporting Si p-i-n wires and one Ni finger (emitter contact) supporting $NiSi_x$ nanowires (NWs). The p-i-n Si wires are grown first by plasma-enhanced chemical vapor deposition (PECVD). The electrical connection between the n^+ layer of these Si wires and the emitter bus is made by the $NiSi_x$ nanowires that are randomly in contact with the Si wires during the course of their growth, in a second CVD step. (b) A scanning electron microscope (SEM) view of a completed device with interdigitated fingers supporting p-i-n Si wires (top) and $NiSi_x$ NWs (bottom). (c) An enlarged SEM view showing the high density of both Si wires and $NiSi_x$NWs on their respective fingers. (d) Another enlarged SEM view showing the high density of contacts between the Si wires and the $NiSi_x$NWs. Figure is adapted from the Ref [38].*

5. SUMMARY AND CONCLUSION

At the current time, radial junction silicon nanowire solar cells has reached the efficiency of ~ 9.2%, this efficiency is similar with thin film solar cells' efficiency based on amorphous silicon (a-Si) and half of bulk c-Si solar cells' efficiency on the market, however this value of efficiency is still low for real application, it needs to be improved more in next time, its stable performance is also an important issue and must be checked thoroughly before coming out to the market. In radial junction SiNW solar cells, Si amount just takes around 10% compare with Si amount in a-Si thin film or bulk c-Si solar cells, this will reduce significantly the cost of SiNW solar cells. With many advantages and be predicted is pioneer structure for real application in the third solar cell generation but radial junction nanowire solar cells fabricated from bottom-up or top-down technique still remains many drawbacks such as low open circuit voltage (V_{oc}) (due to high recombinations rates) and small conversion efficiencies (mostly < 10%). This come from many different reasons such as the low quality of the radial p-n junctions, surface roughness, doping issue, local shunts, metal catalyst impurities, and bad contacts. To achieve high performance SiNWs solar cells, it is necessary to use more "recombination friendly" catalysts for the VLS growth, such as Al, thus reducing deep-level traps in Si, need to improve the quality of p-n junction, we have some various ways such as using a crystalline (ideally single-crystalline) outer shell but this way will take more energy, then the cost, removing defects layer on SiNWs' surface before shell coating is also another way to increase the junction quality. Besides, it is necessary to passivate the NW junction surfaces to reduce the dangling bonds and thus the recombination rate, find out new techniques for top contact to reduce reflection, shadow area, series resistance.

With rapid improvement about the efficiency of the radial junction nanowire solar cells in recent years and this structure was also studied in module for real application, for these backgrounds we are confident that current drawbacks of this structure will be improved and high-performance, low-cost nanowire solar cells will become reality soon and become part of the mainstream industrial photovoltaic technologies.

REFERENCES

[1] Barnham, K. W. J., Mazzer, M. & Clive, B. Resolving the energy crisis: nuclear or photovoltaics? *Nat. Mater.* **5,** 161–164 (2006).

[2] Chapin, D. M., Fuller, C. S. & Pearson, G. L. A New Silicon p ‑ n Junction Photocell for Converting Solar Radiation into Electrical Power. *J. Appl. Phys.* **25,** 676–677 (1954).

[3] Carlson, D. E. & Wronski, C. R. Amorphous silicon solar cell. *Appl. Phys. Lett.* **28,** 671–673 (1976).

[4] King, R. R. *et al.* 40% efficient metamorphic GaInP⁄GaInAs⁄Ge multijunction solar cells. *Appl. Phys. Lett.* **90,** 183516 (2007).

[5] O'Regan, B. & Grätzel, M. A low-cost, high-efficiency solar cell based on dye-sensitized colloidal TiO2 films. *Nature* **353,** 737–740 (1991).

[6] Lee, J. U. Photovoltaic effect in ideal carbon nanotube diodes. *Appl. Phys. Lett.* **87,** 073101 (2005).

[7] Huynh, W. U., Dittmer, J. J. & Alivisatos, A. P. Hybrid nanorod-polymer solar cells. *Science* **295,** 2425–2427 (2002).

[8] Baxter, J. B. & Aydil, E. S. Nanowire-based dye-sensitized solar cells. *Appl. Phys. Lett.* **86,** 053114 (2005).

[9] Cui, Y., Wei, Q., Park, H. & Lieber, C. M. Nanowire Nanosensors for Highly Sensitive and Selective Detection of Biological and Chemical Species. *Science* **293,** 1289–1292 (2001).
[10] Peng, K. *et al.* Aligned Single-Crystalline Si Nanowire Arrays for Photovoltaic Applications. *Small* **1,** 1062–1067 (2005).
[11] Garnett, E. C., Brongersma, M. L., Cui, Y. & McGehee, M. D. Nanowire Solar Cells. *Annu. Rev. Mater. Res.* **41,** 269–295 (2011).
[12] Zhang, Q., Sando, D. & Nagarajan, V. Chemical route derived bismuth ferrite thin films and nanomaterials. *J. Mater. Chem. C* **4,** 4092–4124 (2016).
[13] Misra, S., Yu, L., Chen, W., Foldyna, M. & Cabarrocas, P. R. i. A review on plasma-assisted VLS synthesis of silicon nanowires and radial junction solar cells. *J. Phys. Appl. Phys.* **47,** 393001 (2014).
[14] Peng, K.-Q. & Lee, S.-T. Silicon Nanowires for Photovoltaic Solar Energy Conversion. *Adv. Mater.* **23,** 198–215 (2011).
[15] Abouie, M., Liu, Q. & Ivey, D. G. Eutectic and solid-state wafer bonding of silicon with gold. *Mater. Sci. Eng. B* **177,** 1748–1758 (2012).
[16] Schmidt, V., Wittemann, J. V., Senz, S. & Gösele, U. Silicon Nanowires: A Review on Aspects of their Growth and their Electrical Properties. *Adv. Mater.* **21,** 2681–2702 (2009).
[17] Hsu, C.-M., Connor, S. T., Tang, M. X. & Cui, Y. Wafer-scale silicon nanopillars and nanocones by Langmuir–Blodgett assembly and etching. *Appl. Phys. Lett.* **93,** 133109 (2008).
[18] Peng, K.-Q., Yan, Y.-J., Gao, S.-P. & Zhu, J. Synthesis of Large-Area Silicon Nanowire Arrays via Self-Assembling Nanoelectrochemistry. *Adv. Mater.* **14,** 1164–1167 (2002).
[19] Hasan, M., Huq, M. F. & Mahmood, Z. H. A review on electronic and optical properties of silicon nanowire and its different growth techniques. *SpringerPlus* **2,** (2013).
[20] Cui, Y., Duan, X., Hu, J. & Lieber, C. M. Doping and Electrical Transport in Silicon Nanowires. *J. Phys. Chem. B* **104,** 5213–5216 (2000).
[21] Cui, Y., Zhong, Z., Wang, D., Wang, W. U. & Lieber, C. M. High Performance Silicon Nanowire Field Effect Transistors. *Nano Lett.* **3,** 149–152 (2003).
[22] Choi, S.-Y., Fung, W. Y. & Lu, W. Growth and electrical properties of Al-catalyzed Si nanowires. *Appl. Phys. Lett.* **98,** 033108 (2011).
[23] Moutanabbir, O. *et al.* Colossal injection of catalyst atoms into silicon nanowires. *Nature* **496,** 78–82 (2013).
[24] Garnett, E. & Yang, P. Light Trapping in Silicon Nanowire Solar Cells. *Nano Lett.* **10,** 1082–1087 (2010).
[25] Peng, K. *et al.* Aligned Single-Crystalline Si Nanowire Arrays for Photovoltaic Applications. *Small* **1,** 1062–1067 (2005).
[26] Peng, K. *et al.* Uniform, Axial-Orientation Alignment of One-Dimensional Single-Crystal Silicon Nanostructure Arrays. *Angew. Chem. Int. Ed.* **44,** 2737–2742 (2005).
[27] Peng, K. Q. *et al.* Fabrication of Single-Crystalline Silicon Nanowires by Scratching a Silicon Surface with Catalytic Metal Particles. *Adv. Funct. Mater.* **16,** 387–394 (2006).
[28] Peng, K. *et al.* Metal-particle-induced, highly localized site-specific etching of Si and formation of single-crystalline Si nanowires in aqueous fluoride solution. *Chem. Weinh. Bergstr. Ger.* **12,** 7942–7947 (2006).
[29] Tsakalakos, L. *et al.* Silicon nanowire solar cells. *Appl. Phys. Lett.* **91,** 233117 (2007).
[30] Sivakov, V. *et al.* Silicon Nanowire-Based Solar Cells on Glass: Synthesis, Optical Properties, and Cell Parameters. *Nano Lett.* **9,** 1549–1554 (2009).
[31] Tian, B. *et al.* Coaxial silicon nanowires as solar cells and nanoelectronic power sources. *Nature* **449,** 885–889 (2007).

[32] Gunawan, O. & Guha, S. Characteristics of vapor–liquid–solid grown silicon nanowire solar cells. *Sol. Energy Mater. Sol. Cells* **93,** 1388–1393 (2009).
[33] Putnam, M. C. *et al.* Si microwire-array solar cells. *Energy Environ. Sci.* **3,** 1037–1041 (2010).
[34] Kelzenberg, M. D. *et al.* High-performance Si microwire photovoltaics. *Energy Environ. Sci.* **4,** 866–871 (2011).
[35] Garnett, E. C. & Yang, P. Silicon Nanowire Radial p−n Junction Solar Cells. *J. Am. Chem. Soc.* **130,** 9224–9225 (2008).
[36] Misra, S., Yu, L., Foldyna, M. & Roca i Cabarrocas, P. High efficiency and stable hydrogenated amorphous silicon radial junction solar cells built on VLS-grown silicon nanowires. *Sol. Energy Mater. Sol. Cells* **118,** 90–95 (2013).
[37] Misra, S., Yu, L., Foldyna, M. & Roca i Cabarrocas, P. New Approaches to Improve the Performance of Thin-Film Radial Junction Solar Cells Built Over Silicon Nanowire Arrays. *IEEE J. Photovolt.* **5,** 40–45 (2015).
[38] Toan, L. D. *et al.* Connecting wire-based solar cells without any transparent conducting electrode. *CrystEngComm* **18,** 207–212 (2015).
[39] Al-Ghzaiwat, M. *et al.* Large Area Radial Junction Silicon Nanowire Solar Mini-Modules. *Sci. Rep.* **8,** 1651 (2018).

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