A NOVEL OFFSET FUNCTIONS DESIGN FOR FIVE-LEVEL CASCADE INVERTERS TO REDUCE SWITCHING LOSS

ĐỀ XUẤT HÀM OFFSET GIẢM TỔN HAO DO SỰ CHUYỂN MẠCH CHO NGHỊCH LƯU CASCADE 5 BẬC

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ABSTRACT

This paper presents a new pulse width modulator control method using the offset function to reduce switching loss in five-level Cascade inverter. The proposed technique is based on the offset function being 3rd harmonic voltage. The offset voltage will be added to the control voltages so that the voltage of phase which has absolute of load current largest move into top or bottom of the carriers. So reducing the intersection of control voltage in that phase and the carriers and then reducing the number of switching losses. With the proposed PWM control method, switching loss in a cycle will be decreased. The results of simulations and experiments are provided in order to validate the proposed method. Theoretical, total switching losses applying the proposed technique are 33% lower than standard sine PWM technique. Simulation and empirical results show that applying the proposed algorithm is feasible and meets the ME standards.

Keywords: *Carrier based pulse width modulation; offset function; reducing the number of switching losses; Cascade inverter; five-level.*

TÓM TẮT

Bài báo này trình bày phương pháp điều khiển độ rộng xung (PWM) mới thông qua việc sử dụng hàm offset nhằm giảm tổn hao do sự chuyển mạch của các khóa công suất trong nghịch lưu Cascade 5 bậc. Kỹ thuật đề xuất này sử dụng hàm offset là thành phần áp bậc 3. Điện áp offset được thêm vào điện áp điều khiển sao cho điện áp pha tải có trị tuyệt đối dòng điện là lớn nhất di chuyển lên hoặc di chuyển xuống của sóng mang. Việc giảm giao cắt giữa điện áp điều khiển và sóng mang sẽ giảm số lần chuyển mạch ở vùng tổn hao do sự chuyển mạch nhiều. Với phương pháp điều khiển PWM đề xuất, tổn hao sẽ giảm trong một chu kỳ. Kết quả mô phỏng và thực nghiệm sẽ kiểm chứng cho phương pháp đề xuất. Về mặt lý thuyết, khi áp dụng giải thuật đề xuất tổng tổn hao do sự chuyển mạch giảm 30% so với khi áp dụng kỹ thuật sin PWM tiêu chuẩn. Các kết quả mô phỏng và thực nghiệm cũng cho thấy sự khả thi và đáp ứng các tiêu chuẩn về nhiễm điện từ - ME.

Từ khóa: *Điều chế sóng mang; hàm offset; giảm số lần chuyển mạch; nghịch lưu Cascade; 5 bậc.*

1. INTRODUCTION

Multilevel inverters are power electronic converters that play important roles in applications of mechanical-electrical systems, transportation, power quality management, renewable energy conversion such as solar energy, wind energy connected to electrical grids. Space-vector pulse width modulation and carrier based pulse width modulation are the typical control techniques of inverters [1]-[3]. Because of industrial requirements, the inverters made with the capacity greater than [4]. Due to the increase in capacity of the inverters, the power loss becomes a problem that needed to solve.

It causes power losses in inverter including a loss in power source (P_S), loss in wires (P_L), loss in control circuit (P_{Dr}), and loss in switches (P_{SW}) [5]. Of the power losses mentioned above, loss in switches is the largest, depending on modulation algorithm and topology [6]. The loss on switches of the inverter on a period of control voltage can be determined as (1):

$$P_{SW} = P_{SS} + P_{CS} \quad (1)$$

Where P_{CS} and P_{SS} are conductive and switching loss of switches.

$$P_{SS} = \sum_{i=1}^{p} P_{S,i} \quad (2)$$

$P_{S,i}$ is switching loss on the i^{th} switch; p are number of switches in topology.

According to [7], the switching loss on the i^{th} switch ($P_{S,i}$) depends on the number of switching in a control voltage cycle and is determined by the formula (3).

$$\mathbf{P_{S,i}} = \sum_{\mathbf{i=1}}^{\mathbf{n}} \mathbf{E_{ON} \cdot V_{CEi} \cdot I_{Ci}} + \sum_{\mathbf{j=1}}^{\mathbf{m}} \mathbf{E_{OFF} \cdot V_{CEj} \cdot I_{Cj}} \quad (3)$$

Where n is the number of times of status changed from OFF to ON; m is the same from ON to OFF. E_{ON} and E_{OFF} are the energies for switching ON and OFF, respectively. V_{CEi} and I_{Ci} are the voltage across power switch before conducting and the current after conducting at ON state i, respectively; V_{CEj} and I_{Cj} are the voltage across power switch after being OFF and the current before being OFF conducting at OFF state j, respectively.

Because V_{CEi}, $V_{CEj,}$ and supply voltage are equal, so that, reducing the switching or the switching takes place at a smaller of I_C, it will reduce switching losses. There is the base of the algorithm to reduce switching loss. The study [7] shows reducing switching frequency often has the side effect is increased THD, so content paper proposes a new modulation technique reduces the number times of the switching on the phase that absolute of load current value is maximum. The proposed algorithm based on the use of the offset function put voltage control (which has a maximum of absolution load current) on the top or bottom level of the carrier. Because the duration of each phase, reaching its absolute of load current on maximum, are the same and equal 1/3 cycle of the control voltage, the number of switching will decrease to about 33 percent. Proposed algorithm will be simulated and experimental by PSIM with the help of a laboratory prototype.

2. TOPOLOGY OF FIVE-LEVEL CASCADE INVERTERS

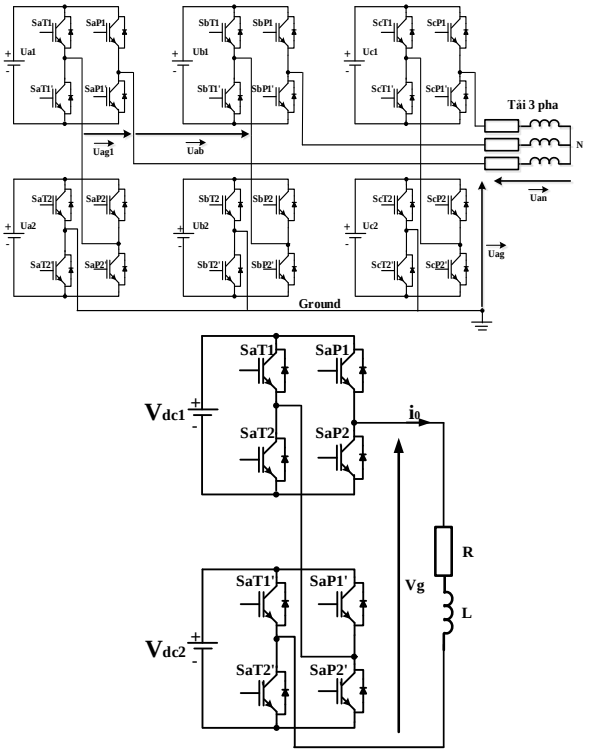


***Figure 1**. Five-level Cascade inverter.*

Structure of a phase of five level Cascade inverter is in figure 1 [8]. Hence, the voltage from phase to pole (U_{xgj}) is determined by (4):

$$U_{xgj} = (T_{Sxj}).U_{xj} = (T_{SxTj} - T_{SxPj}).U_{xj} \quad (4)$$

Where T_{Sxch} is defined in (5) with Ch=T, P (showed by left side branch and a right side branch, respectively).

$$T_{Sxj} = T_{SxPj} - T_{SxTj} \quad (5)$$

Where j is the index of switches (1 to 4) and T is the state of the switch.

So, the phase to pole voltages is given by (6):

$$\begin{bmatrix} U_{ag} \\ U_{bg} \\ U_{cg} \end{bmatrix} = u \begin{bmatrix} T_{Sa} \\ T_{Sb} \\ T_{Sc} \end{bmatrix} \quad (6)$$

The phase voltages and line to line voltages of five-level Cascade inverter is given by (7) and (8):

$$\begin{bmatrix} U_{an} \\ U_{bn} \\ U_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} U_{ag} \\ U_{bg} \\ U_{cg} \end{bmatrix} \quad (7)$$

$$\begin{bmatrix} U_{ab} \\ U_{bc} \\ U_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} U_{an} \\ U_{bn} \\ U_{cn} \end{bmatrix} \quad (8)$$

Thus, phase to pole voltages U_{xg} and line to line voltages U_{xy} have the third order harmonic while the phase voltage U_{xn} do not. Therefore, it can be seen that if the offset function in the proposed algorithm of inverter control which is the third order harmonic will not affect the magnitude of the third order harmonic of the load. Besides, the phase to pole voltage U_{xg} will have 5 level including two positive levels, two negative levels and zero. There are ±2U, ±U, and 0.

3. CARRIER PWM ALGORITHM TO REDUCE THE NUMBER OF SWITCHING

This CPWM algorithm proposed in [9]. The main idea in this algorithm is to add a third order harmonic, called offset voltage, to control signal, with the aim of reducing the switching of the leg phase has a difference between the control voltages and nearest carriers is the smallest. Call v_x is voltage to control x phase, and v_{rx} is calculated to control voltage from the PWM modified algorithm to reduce switching frequency. The principle of this algorithm was shown in Fig 2 [9].

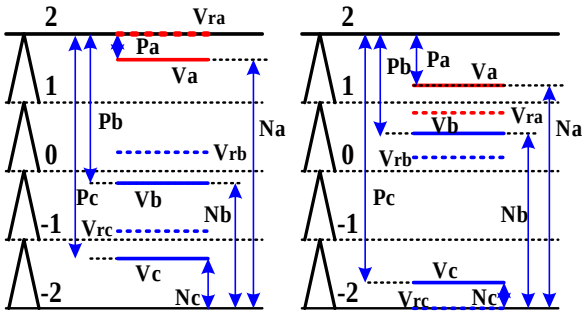


Figure 2. *Principle of the CPWM algorithm to reduce the number of switching [9]*

The simulation results show that this algorithm allows reducing the switching of the leg phase that different of control voltages of it with the nearest carrier is smallest. Therefore switching can do on the phase that has load current (absolute) being smallest. So switching loss is not minimums. Then it is necessary for the proposed algorithm to reduce switching in the phase which loads current (I_C) none smallest. This is the ideal solution to reduce energy losses due to switching without sacrificing THD as prescribed.

4. PROPOSED ALGORITHM

4.1. The principle of algorithm

On 3-phase five-level Cascade inverter, because the voltage across the switchV_{CEi} and V_{CEj} is always U_{DC} / 2, so the switching loss depends on the current through power switches and the number of switching in the period of the control voltage. Thereby reducing the switching on the phase has maximum (priority first-if can) or medium (priority second) of absolution load current. Define: v_x is control voltage initial phase x, v_{rx} is calculate to control voltage from the algorithm. Select 0 is the bottom of the carrier with the smallest amplitude and peak amplitude of the triangle carrier waves are equal and equal to 1, then this time the threshold comparison of the carrier will be 0, 1, 2, 3 and 4. The control voltage of phase x is v_x is determined by (9).

$$v_x = v_{1,x} \cos(\omega t + j_x) + 2 + v_{offset} \quad (9)$$

Define L_x and ε_x as follows:

$$L_x = \begin{bmatrix} int(v_x)\ if\ int(v_x) < 4 \\ int(v_x) - 1 \quad else \end{bmatrix} \quad (10)$$

$$e_x = v_x - L_x \quad (11)$$

Call I_{xABS} is the absolute value of current across phase x.

And define the matrixes as (12 to 17)

$$[I_{max}] = [amax, \quad bmax, \quad cmax] \quad (12)$$

$$xmax = \begin{cases} 1\ if\ I_{xABS} = \max(I_{aABS}, I_{bABS}, I_{cABS}) \\ 0\ else \end{cases}$$

$$[I_{min}] = [amin, \quad bmin, \quad cmin] \quad (13)$$

$$xmin = \begin{cases} 1\ if\ I_{xABS} = \min(I_{aABS}, I_{bABS}, I_{cABS}) \\ 0\ else \end{cases}$$

$$[I_{med}] = [amed, \quad bmed, \quad cmed] \quad (14)$$

$$xmed = 1 - xmax - xmin$$

$$[E_{max}] = [eamax, \quad ebmax, \quad ecmax] \quad (15)$$

$$exmax = \begin{cases} 1\ if\ e_x = \max(e_a, e_b, e_c) \\ 0\ else \end{cases}$$

$$[E_{min}] = [eamin, \quad ebmin, \quad ecmin] \quad (16)$$

$$exmin = \begin{cases} 1\ if\ e_x = \min(e_a, e_b, e_c) \\ 0\ else \end{cases}$$

$$[E_{med}] = [eamed, \quad ebmed, \quad ecmed] \quad (17)$$

$$exmed = 1 - exmax - exmin$$

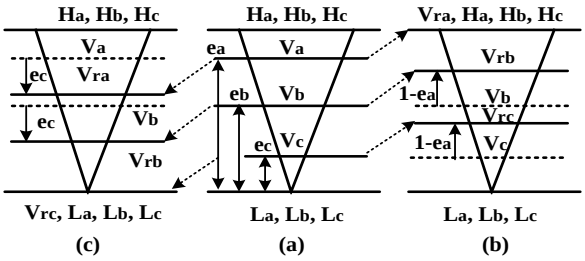


Figure 3. *Principle of the proposed algorithm*

So that with v_a, v_b, and v_c showed in fig 3a, there are four cases and then we can decide offset voltage as in table 1

Table 1. *Conditions and selected offset voltage*

Case	Conditions	Fig	Offset
1	amax=1; eamax=1	3b	1-e_a
2	cmax=1; ecmin=1	3c	-e_c
3	bmax=1; ebmed=1; amed=1	3b	1-e_a
4	bmax=1; ebmed=1; cmed=1	3c	-e_c

So general offset function is determined as (18).

$$v_{offset} = -e_{min}.([I_{max}].[e_{min}]^T + [I_{max}].[e_{med}]^T.[I_{med}].[e_{min}]^T) + (1 - e_{max}).([I_{max}].[e_{max}]^T + [I_{max}].[e_{med}]^T.[I_{med}].[e_{max}]^T) \quad (18)$$

The control voltage (v_{rx}) after added offset will move to the new location inside phase has a minimum of offset and the absolute value of the load current being maximum or medium. (Figure 4).

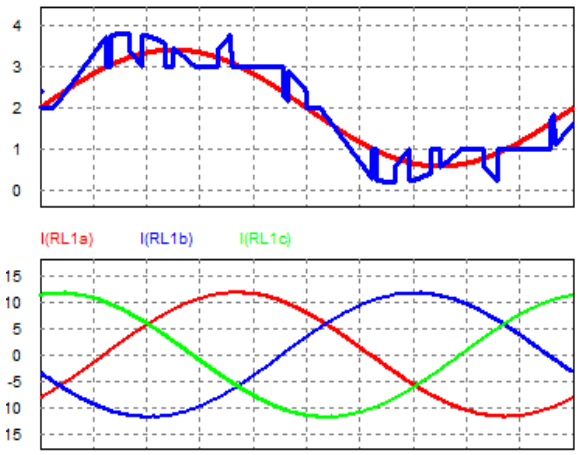


Figure 4. *Controlled Voltage initially and after applied the proposed algorithm m=0.9.*

Formula (18) may seem complicated, but the elements of the matrixes are only valid "0" and "1" so the calculation will be very fast and easy.

4.2. Flow chart

From 4.1.1, the flow chart of proposed algorithm built as figure 5. The flow chart shows that the proposed algorithm uses simple commands as a plus, minus, comparison of the program.

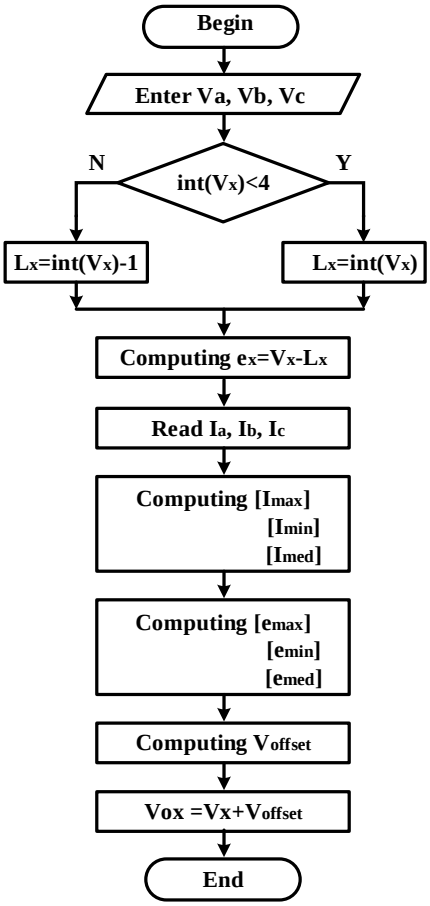


Figure 5. *The proposed flow chart*

The comparison of the phase currents can be done by comparing circuits (hardware and does not require the use of expensive sensors). Thus, calculation time is low, suitable for closed-loop control or other control methods.

5. SIMULATION AND EXPERIMENTAL RESULTS.

Table 2 *Parameters Used in Simulation and Experiment*

Parameter/Component		Attributes
Input voltage	V_{dc}	100 V
Desired output phase voltage	V_{ph}	200 Vrms
Output frequency	f_o	50 Hz
Carrier frequency	f_s	10 kHz
Modulation index	m	0.9
Capacitors	$C_1 = C_2$	4700 µF/300 V
Three-phase RL load	R_{load},-L_{load}	40 Ω-20mH

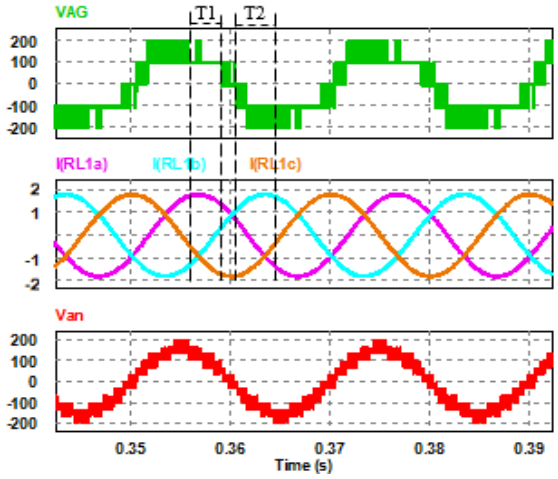
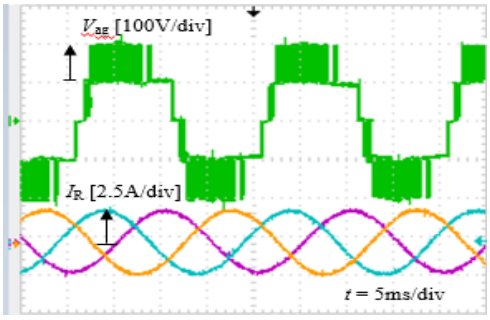
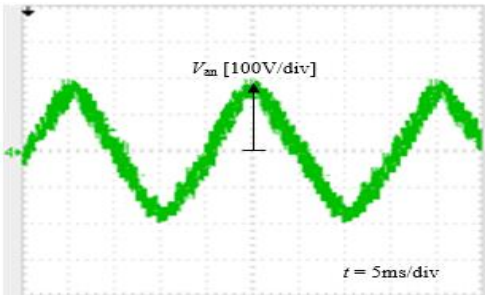


Figure 6. *Simulation results of the proposed algorithm*



a)



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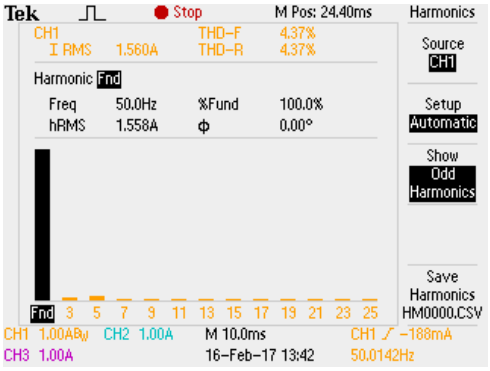

c)

Figure 7. *Experimental results of the proposed algorithm.*

Figure. 6 shows the simulation results of the proposed algorithm when Vdc = 100 V and m = 0.9. As shown in Fig. 6, the top waveform is the pole voltage (Vag) has five levels: 200 V, 100 V, 0 V, -100 V and −200 V, the middle waveform is the three-phase output current equal 1.6 A and the bottom waveform is output phase voltage V_{an}. The simulation results show that when the absolute of phase current "A" reach maximum (some time medium) – T_1, then switching on the phase is lower than it when phase current near zero (T_2).

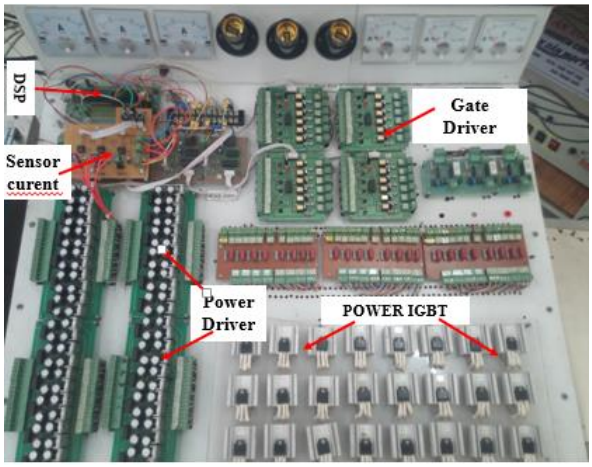

Figure 8. *A laboratory prototype of the proposed algorithm.*

A prototype based on the DSP TMS320F28335 microcontroller is built in the laboratory to verify the effectiveness of the proposed PWM control technique. Fig. 8 presents a photograph of the laboratory prototype. The input voltage is 100 V. The desired RMS output phase voltage is 200 V. The output frequency is 50 Hz. The switching frequency of the inverter circuit is 10 kHz. All FGL40N150D IGBTs in the prototype are controlled by TLP250 amplifiers. The modulation index in the proposed algorithm is 0.9.

In Figure. 7(a) the pole voltage (Vag) and the three-phase output current, Figure. 7(b) output phase voltage Van and Figure. 7(c) shows the harmonics of the load current.

Compares the values of the voltages from the simulation and experimental results of the proposed algorithm. The simulated values are close to the measured values. The proposed algorithm reduces the switching about 30%. So certainly, losses due to the switching will be smaller too. The total harmonic distortion (THD%) of phase current go respectively 4.37%.

6. CONCLUSIONS

The paper presents the carrier based pulse width modulation algorithm by using offset function to reduce the number of commutations of power switches in Cascade five-level inverters special reduced switching positions of the phase having a maximum of absolute of phase current, therefore, the proposed algorithm can reduce switching losses. This algorithm can not only reduce the number of switching, but also select phase having larger current for reducing of switching. A laboratory prototype was constructed to demonstrate the operating principle of the proposed algorithm. Simulations and experimental results confirmed the accuracy of the theoretical analysis.

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