LOW POWER CAM MEMORY DESIGN USING POWER GATING TECHNIQUE

THIẾT KẾ BỘ NHỚ CAM CÔNG SUẤT THẤP DÙNG KỸ THUẬT POWER GATING

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ABSTRACT

In this paper, the author has designed and simulated low-power CAM memory. Content address memory (CAM) will compare stored data with search data and return the appropriate address. CAM is used in applications of packet forwarding and packet sorting in network routers. The article designates a conventional CAM memory and a proposed CAM memory. The proposed CAM memory is designed to reduce overall energy consumption. The proposed CAM memory is designed using power gating technique to cut off the consumption current during CAM data comparison. In addition, this study applies proposed CAM memory to design parity bit checker to reduce delay and consumption power. The author uses Cadence software to perform conventionally and proposed CAM simulations to find the results in comparing those two memories. Based on the results of the simulation, the match-line current is reduced by 59.3%, the delay time is reduced by half and the proposed CAM leakage current is reduced by 96.6% compared to conventional CAM in 45nm CMOS technology.

Keywords: Content addressable memory (CAM); Match line; Bit Parity; Power gating; Low power.

TÓM TẮT

Trong bài báo này tác giả thực hiện thiết kế và mô phỏng bộ nhớ CAM công suất thấp. Bộ nhớ địa chỉ nội dung (CAM) sẽ so sánh dữ liệu lưu trữ với dữ liệu tìm kiếm rồi trả về địa chỉ phù hợp. CAM được sử dụng nhiều trong ứng dụng của chuyển tiếp gói tin và phân loại gói tin trong các bộ định tuyến mạng. Bài báo thiết kết một bộ nhớ CAM thông thường và một bộ nhớ CAM đề xuất. Nghiên cứu tiến hành thiết kế bộ nhớ CAM đề xuất với mục đích nhằm giảm năng lượng tiêu thụ cho toàn mạch. Bộ nhớ CAM đề xuất đã được thiết kế dùng kỹ thuật power gating nhằm ngắt dòng tiêu thụ trong quá trình so sánh dữ liệu của CAM. Bên cạnh đó, nghiên cứu áp dụng bộ nhớ CAM này vào thiết kế bộ kiểm tra bit Parity nhằm giảm được thời gian trì hoãn và công suất tiêu thụ. Tác giả đã sử dụng phần mềm Cadence thực hiện mô phỏng CAM thông thường và CAM đề xuất để tìm ra kết quả so sánh hai bộ nhớ đó. Dựa trên kết quả mô phỏng tác giả đã thấy dòng matchline đã giảm được 59.3%, thời gian delay đã giảm được một nửa và dòng rò của CAM đề xuất đã giảm được 96.6% so với CAM thông thường trong công nghệ CMOS mô phỏng 45nm.

Từ khóa: *Content addressable memory (CAM); Match line; Bit Parity; Power gating; Low power.*

1. INTRODUCTION

Content-addressable memory (CAM) is a special kind of computer memory used in high-speed search applications. CAM is made up of conventional semiconductor memory, SRAM, with a comparator circuit that can allow a complete search operation in the same cycle. CAM compares the input search data with a stored data table and

returns the address of the matched data. The two most popular intensive search tasks that use CAM are packet forwarding and packet sorting in Internet routers [1].

Since the CAM simultaneously searches for the entire memory cell to recognize the contents of the matching signal, the memory array is accessed and compared in parallel. This parallel implementation consumes considerable power. This makes the implementation of CAM memory limited to many applications. Consequently, reducing power consumption is a key decision criterion when designing CAM memory in addition to area saving criteria and achieving high performance of CAM memory. Many studies have proposed different circuit diagrams to reduce CAM memory consumption power [2-6]. Here, CAM can be designed with additional circuitry to turn off the power supply to reduce the consumption current in case of inactivity CAM [2]. Parallel comparison processes are performed by using Pipeline techniques to reduce power [3] or using a Segmented Match Line [4-5], or using low-power transistor technology [6].

In the proposal of this study, the author uses power gating techniques, which are often applied in digital circuits to control the reduction of current consumption when the circuit is going to idle state [7] to reduce power consumption. In this paper, the power gating technique is used to turn off the power supply when the search process does not find the data stored.

2. CAM MEMORY STRUCTURE

CAM memory operates in three modes: read, write and compare [1]. Figure 1 is a block diagram of a Normal CAM. SL and NotSL signals are the search lines of CAM. Nodes of A and B are storing data. Transistors M1, M2, M3 and M4 form a comparator in principle of logic-based XNOR. ML is the match line that represents the result of the comparison process.

The basic principle of CAM operations is usually divided into three phases: SL Pre-charge, ML Pre-charge and ML Evaluation. Fig. 2 shows a CAM three-stage timing diagram. First, during the pre-charge of the SL, the SL signal is charged to a high level of V_{DD}. The ML signal will be pulled down to a low level of 0 V at the ML pre-charge stage. When the ML evaluation is performed, the SL and NotSL signals are re-established and the comparison process starts at the ML evaluation stage.

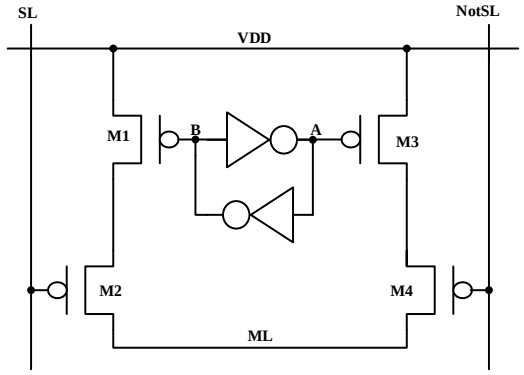

Figure 1. *Block diagram of a normal CAM.*

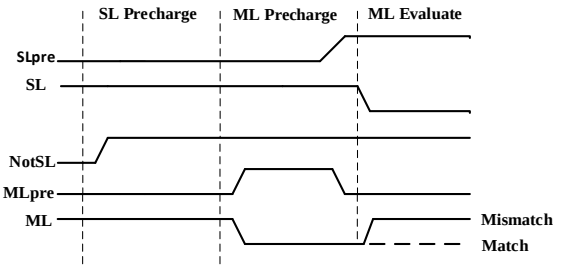

Figure 2. *Three matchline evaluation stages*

When data is not found in the CAM Cell (for example, SL = "0"; NotSL = "1" and A = "1"; B = "0") then transistors M1 and M2 will be switched on and ML will be charged to power that voltage near V_{DD} as shown in figure 2. If these transistors are not conducted, the ML will remain at its initial low state when the ML precharge has set the status level for ML as shown in figure 2.

3. PROPOSED CAM MEMORY

The structure of a proposed CAM is shown in Figure 3. The suggested CAM memory still includes SRAM memory and comparator circuits same as conventional CAM. However, proposed CAM memory will be allocated by two separate power rails, V_{DDML} and V_{DD}. The V_{DDML} power rail will be controlled by the P_X transistor and the

previous feedback loop. The V_{DD} power rail will be allocated to the SRAM memory while the V_{DDML} power will be allocated to the comparator circuit to save energy during the comparison process. This is because the CAM dissipates the largest power while the comparison process takes place.

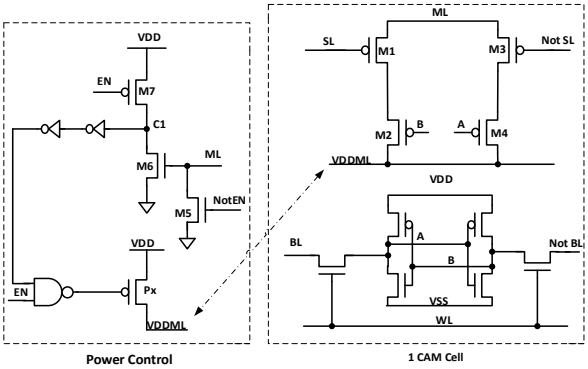

Figure 3. *Block diagram of a proposed CAM*

In Figure 3, we see that the V_{DDML} voltage supply control circuits for CAM memory operation are as follows: First, the EN signal is low-level, transistor M7 is ON. Then, NAND gate output is a 1-level, transistor Px is OFF then ML is low. When the EN is high, the transistor Px is ON. The V_{DDML} voltage is supplied and the comparator process begins in the CAM. When the mismatch occurs, the ML voltage will start to be charged. Here, all CAM cells will share the power rail of the V_{DDML} power for any mismatch. The charge process occurs until ML reaches the threshold voltage value of transistor M6. At this time, M6 begins to turn ON and pulls C1 down to the ground, and shuts down the V_{DDML} power. The charge-up process takes place in a short time, resulting in a dramatic drop in consumption power. This is the power saving technique of the proposed CAM.

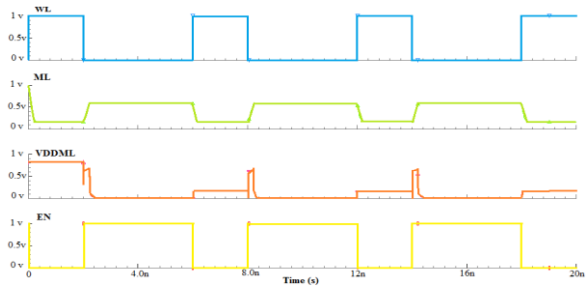

Figure 4. *Showing the simulated signal of proposed CAM with 1 mismatch*

Figure 4 is the simulation result of a proposed CAM in case of a mismatch. Cadence software has been used to simulate this CAM memory. CAM cells have been designed using 45nm CMOS technology. From figure 4 we can see that the "EN" signal is high, the comparison process takes place and the ML voltage is only a half V_{DD} as shown above.

4. APPLICATION OF PARITY BIT CHECKER DESIGN USING PROPOSED CAM MEMORY.

Applying proposed CAM memory to even bit parity checker improves comparability by eliminating unsuitable data quickly based on comparisons between the parity bits of the search data and storage data. As a result, data are searched faster, improving productivity. The parity bit is added to the increase in the ability of mismatch data.

Figure 5. *Data table for 8 CAM cells in simulations*

The eight bits based on the CAM design shown in figure 5 consist of 7 data bits and a parity bit. This parity bit will depend on the number of bits "1" on each data line. As shown in Figure 5, row ML1 and row ML2 show a parity bit of "0" as the result since we have total CAM cells that store "1" bit as even. At line ML3, the parity bit is "1" because the total number of bits "1" stored in the CAM cells is odd.

The comparative search operation in the parity bit checker is as follows: First, the checker will compare between store data and search data, considering whether the two data are matched or not. If one of the bits does not match each other, the data are mismatched. For example, in the figure, the parity bit of

the ML3 line is different from the bit parity of the search data, so the search data line only compares with the bits in the ML1 and ML2 lines. Next, the checker compares the "1" and "0" bits of both ML1 and ML2 to find the appropriate data.

5. COMPARISON RESULTS BETWEEN CONVENTIONAL CAM AND PROPOSED CAM.

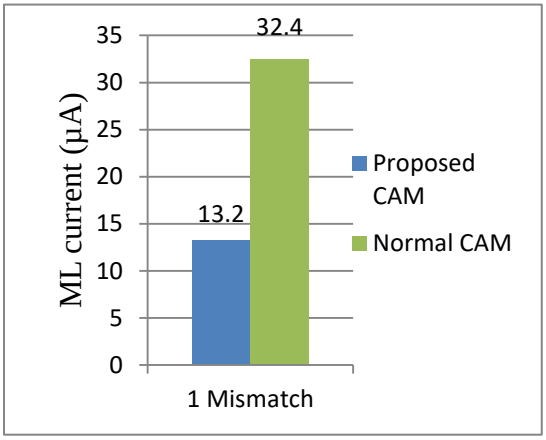

Figure 6. *Matchline lines of normal CAM and proposed CAM.*

Match-line current determines whether the stored data and search data are matched or mismatched. Figure 6 shows the simulation results. We can see that the ML current is reduced to 59.3% compared to normal CAM in case one mismatch. This is because the proposed CAM memory is designed to add a power control circuit that uses energy-saving power gating. The additional power circuit is used to control the voltage value so that the V_{DDML} voltage is limited only about half the V_{DD} voltage.

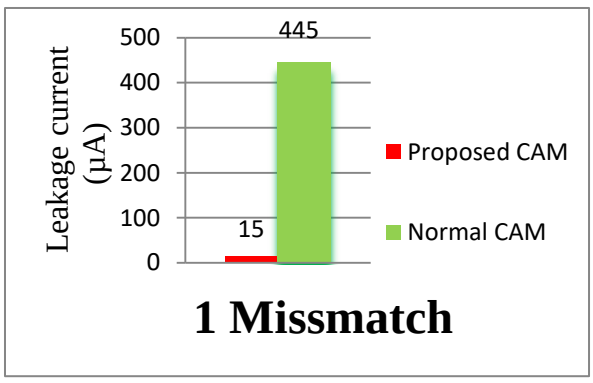

Figure 7. *Leakage current of normal CAM and proposed CAM*

Leakage current through the parity checker is the average current of the V_{DD} supply power, which is characteristic of the energy loss across the circuit. Figure 7 shows very large differences between the conventional CAM and the proposed CAM, in term of leakage current. The proposed CAM circuit leakage consumes very small total power. This is because the proposed CAM cuts off the power supply rail when the circuit falls into the mismatched data state. Here, the consumption current is the sum of parity checker current.

Sensing delay is an important metric in evaluating CAM memory operability. In a work cycle, the Match-line Signal (ML) confirms the current data whether it is true or false. The CAM memory delay value is calculated from the start time of the comparison phase until the end of the comparison phase. From the results of the figure 8 we find that the proposed CAM delay is only a half the normal CAM delay in case of one mismatch, which is the worst case comparison of the design timing. Here, power gating is used by inserting a PMOS transistor into power rail, there is a small voltage drop on this switching PMOS transistor compared to non-power gating circuits [7]. However, this drop voltage causes a negligible delay overhead on the proposed CAM. It is because the proposed CAM's ML signal is only a half the ML voltage of the conventional CAM during the comparison process, so proposed CAM's delay time is faster than the conventional CAM.

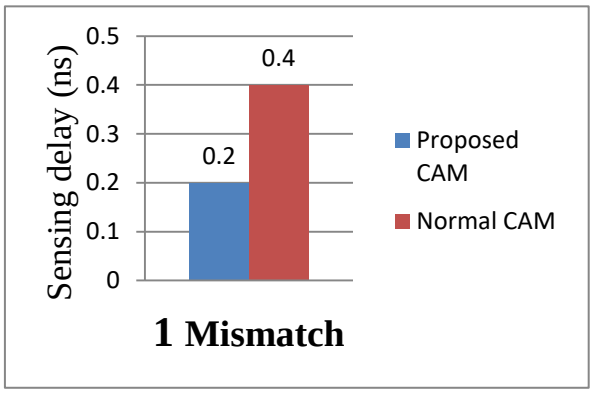

Figure 8. *Sensing delay of normal CAM and proposed CAM*

From the results of Figure 9, we can see that the more mismatches occur, the more voltage on the ML is charged faster and the time delay is less. Proposed CAM delay time is less than the normal CAM.

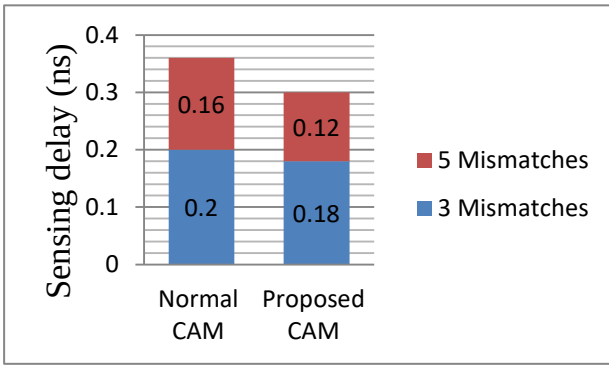

Figure 9. *Sensing delay of normal CAM and proposed CAM in different mismatch cases.*

6. CONCLUSION

The author designed the extra circuit to reduce the consumption power of the CAM during the comparison process. The study applies this technique to the bit parity checker to evaluate the comparison results of the proposed CAM memory with conventional CAM memory in term of sensing delay and power dissipation. The obtained results show the match-line current is reduced by 59.3%, the delay time is reduced by a half and the proposed CAM leakage current is reduced by 96.6%.

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