PULSE-WIDTH MODULATION STRATEGY FOR COMMON MODE VOLTAGE ELIMINATION IN THREE-LEVEL NEUTRAL POINT CLAMPED INVERTERS WITH REDUCED COMMON MODE VOLTAGE SPIKES

KỸ THUẬT ĐIỀU CHẾ ĐỘ RỘNG XUNG CHO TRIỆT TIÊU ĐIỆN ÁP COMMON MODE KẾT HỢP VỚI GIẢM GAI CHO NGHỊCH LƯU BA BẬC DIODE KẸP

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ABSTRACT

This paper presents a pulse-width modulation strategy for common mode voltage elimination in the three-level neutral point clamped (NPC) inverter with reduced common mode voltage spikes. The strategy utilizes the three zero common mode voltage vectors in the space vector diagram and is implemented by using a carrier-based pulse-width modulation (PWM) technique. Based on the use of three zero common mode voltage vectors, the two PWM patterns can be derived, describing the base voltages and average active switching voltages of the three phases in one sampling period. The common mode voltage spikes are partly due to the deadtime which is mandatory in the real-world switching conditions to avoid shoot-through in the inverters. Hence, the impact of deadtime is analyzed in detail. By taking the deadtime effect into account, the proposed method is capable of reducing spikes in common mode voltage waveform. Simulation and experimental results verify the effectiveness of the strategy.

Keywords: *Spikes; Common Mode Voltage; Deadtime; Pulse-Width Modulation (PWM); Neutral Point Clamped (NPC).*

TÓM TẮT

Bài báo trình bày phương pháp điều chỉnh độ rộng xung để triệt tiêu điện áp common mode cho nghịch lưu ba bậc diode kẹp kết hợp với việc giảm gai cho điện áp common mode. Phương pháp sử dụng ba vector điện áp common mode bằng 0 trong sơ đồ vector không gian và thực hiện hóa bằng phương pháp song mang. Dựa vào việc sử dụng ba vector common mode bằng 0, hai mẫu điều chế độ rộng xung được suy ra, mô tả điện áp nền và điện áp đóng cắt trung bình của ba pha trong một chu kỳ lấy mẫu. Ảnh hưởng của thời gian chết được khảo sát chi tiết. Do đó, dựa vào ảnh hưởng của thời gian chết phương pháp trình bày trong bài báo này có khả năng giảm gai cho điện áp common mode. Mô phỏng và thực nghiệm kiểm chứng sự hiệu quả của phương pháp.

Từ khóa: *Gai; Điện áp Common mode; Thời gian chết; Phương pháp điều chỉnh độ rộng xung; Ba bậc diode kẹp.*

1. INTRODUCTION

Multilevel inverters are increasingly popular in motor-drive applications. Two well-known multilevel inverters include a diode-clamped inverter and cascaded inverter. As regards the control techniques for these two types of multilevel inverters, the space vector modulation (SVPWM), carrier-based pulse-width modulation

(CBPWM), and selective harmonics elimination (SHE) are used. Compared to a conventional two-level inverter, multilevel inverters have several advantages such as low total harmonics distortion and high blocking voltage, which are suitable for medium voltage drive applications. However, the common mode voltage which is responsible for the bearing failure, thereby reducing the life expectancy of motors still exists in multilevel inverters. Moreover, the common mode voltage also leads to electromagnetic interference (EMI), which in turn results in the improper operation of nearby working devices. Therefore, it should be reduced or eliminated by either hardware or software solutions. On a hardware front, extra hardware is included, thereby increasing the volume and cost of the system. Multilevel inverters, especially the three-level neutral point clamped inverter is capable of reducing or eliminating the common mode voltage thanks to a large number of switching voltage states as opposed to a conventional two-level inverter. Papers in [1], [2] attempt to reduce the common mode voltage by avoiding some switching voltage vectors that cause large common mode voltage magnitudes while other authors in [3], [4] propose pulse-width modulation strategies for complete common mode voltage elimination by neglecting all voltage vectors responsible for generating the common mode voltage. However, the spikes in common mode voltage waveform still occur partly due to the impact of the deadtime. Therefore, this paper presents a carrier-based pulse-width modulation method to eliminate the common mode voltage in the three-level neutral point clamped inverter with spikes reduction by taking the deadtime effect into account. The impact of deadtime is investigated in detail and the modulation strategy is then proposed. Simulation and experimental results verify the effectiveness of the proposed method.

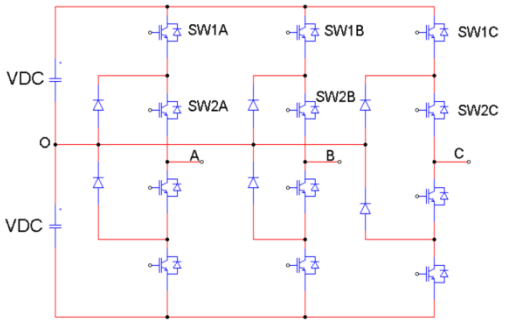


Figure 1. *The Three-Level Neutral Point Clamped Inverter.*

2. PULSE-WIDTH MODULATION STRATEGY TO ELIMINATE CMV IN THREE-LEVEL NPC INVERTERS [5]

In the three-level neutral point clamped inverter under the balanced DC-link voltages, the pole voltage of X phase (X∈ A, B, C) can be represented as:

$$V_{XO} = (s_{1X} + s_{2X})V_{DC} - V_{DC} \quad (1)$$

Where: s_{1X}, s_{2X} are the switching states of SW_{1X}, SW_{2X} respectively. If s_{1X} is 1, then SW_{1X} is ON. If s_{1X} is 0, then SW_{1X} is OFF.

The component $(s_{1X} + s_{2X})V_{DC}$; X∈ $\{A, B, C\}$ in (1) is called the switching voltage. The normalized switching voltage can be then defined as:

$$V_{Xn} = s_{1X} + s_{2X} \quad (2)$$

The normalized switching voltage has another form based on the relationship between the switching voltage and the pole voltage V_{XO}:

$$V_{Xn} = \frac{V_{XO}}{V_{DC}} + 1 \quad (3)$$

The normalized switching voltage V_{Xn} can be decomposed into 2 components.

$$V_{Xn} = L_X + s_X \; ; X \in \{A, B, C\} \quad (4)$$

Where: L_X is the base voltage of V_{Xn} and s_X is the active switching component of V_{Xn}. s_X can be 0 or 1 while L_X can have values of 0 or 1 in the three-level NPC inverter.

The average value of V_{Xn} in one sampling period can be expressed as:

$$v_{Xn} = L_X + \varepsilon_X \; ; \; 0 \le \varepsilon_X \le 1 \quad (5)$$

Where: L_X is the base voltage of phase X (X∈ A, B, C) and a constant number in a sampling period. ε_X is the average active switching value of s_X in a sampling period.

If v_{Xl}^*, X∈ $\{A, B, C\}$ is defined as the reference load voltage, v_{Xn} in (5) can also be expressed as:

$$v_{Xn} = \frac{v_{Xl}^*}{V_{DC}} + v_{off}^* \quad (6)$$

The offset voltage v_{off}^* can have any values between the lower and upper limits defined as:

$$v_{off\_min} = -\frac{Min}{V_{DC}} \le v_{off}^* \le v_{off\_max} = 2 - \frac{Max}{V_{DC}} \quad (7)$$

Where: Max and Min are the maximum and minimum values of the three reference load voltages ($v_{Al}^*, v_{Bl}^*, v_{Cl}^*$) in one sampling period.

The common mode voltage defined for the three-level NPC inverter is expressed as:

$$V_{CM} = \frac{V_{AO}+V_{BO}+V_{CO}}{3} \quad (8)$$

From (3), the instantaneous common mode voltage V_{CM} in (8) can be written as:

$$V_{CM} = \frac{(V_{An}+V_{Bn}+V_{Cn}-3).V_{DC}}{3} \quad (9)$$

In order for the common mode voltage to be zero, the sum of $V_{An}, V_{Bn}, and\ V_{Cn}$ has to be equal to 3. In terms of the average values of V_{An}, V_{Bn}, V_{Cn}, the zero CMV leads to the condition $v_{off}^* = v_{off,ZCMV} = 1$ provided that $v_{Al}^* + v_{Bl}^* + v_{Cl}^* = 0$.

Let us define F, F_l, F_e as the total switching voltage, total base voltage, and total active average switching voltage, respectively.

$$F = F_L + F_e \quad (10)$$

$$F_L = L_A + L_B + L_C \quad (11)$$

$$F_e = \varepsilon_A + \varepsilon_B + \varepsilon_C \quad (12)$$

$$L_X = \begin{cases} Int(v_{Xn})\ if\ v_{Xn} < 2 \\ 1\ if\ v_{Xn} = 2 \end{cases}; 0 \le L_X \le 1 \quad (13)$$

$$\varepsilon_X = v_{Xn} - L_X \quad (14)$$

Where: $Int(v_{Xn})$ function returns the smallest integer value of v_{Xn}.

For zero CMV condition, there are two possible cases expressed as follows:

$F_L = 1;\ F_e = 2$

$F_L = 2;\ F_e = 1$

The two-active voltage hexagonal diagrams corresponding to ($F_L = 1$ & $F_e = 2$) and ($F_L = 2$ & $F_e = 1$) are shown in Fig. 2.

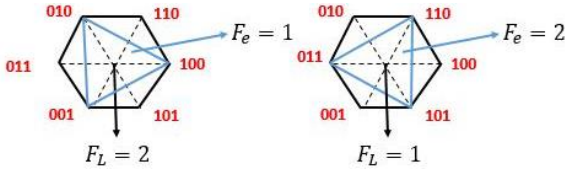


Figure 2. *Active voltage hexagonal diagrams of ($F_L = 2$ & $F_e = 1$) and ($F_L = 1$ & $F_e = 2$) [5].*

With the aid of the base voltages (L_A, L_B, L_C), the reference voltage in the three-level NPC inverter can be synthesized by a virtual carrier-based PWM pattern similar to a two-level PWM one. The two virtual standardized PWM patterns corresponding to ($F_L = 1$ & $F_e = 2$) and ($F_L = 2$ & $F_e = 1$) are illustrated in Fig. 7.

For each virtual standardized pattern, there are six possible mapping functions which are shown in Table 1. Selecting which mapping function depends upon the control purpose.

Table 1. *Possible mapping function and modulating signals determination [5]*

$A \to d$ $B \to s_1$ $C \to s_2$	$A \to d$ $B \to s_2$ $C \to s_1$	$A \to s_1$ $B \to d$ $C \to s_2$	$A \to s_2$ $B \to d$ $C \to s_1$	$A \to s_1$ $B \to s_2$ $C \to d$	$A \to s_2$ $B \to s_1$ $C \to d$
ε_1=ε_B ε_2=ε_C	ε_1=ε_C ε_2=ε_B	ε_1=ε_A ε_2=ε_C	ε_1=ε_C ε_2=ε_A	ε_1=ε_A ε_2=ε_B	ε_1=ε_B ε_2=ε_A

The block diagram of the complete CMV elimination PWM method is demonstrated in Fig. 3.

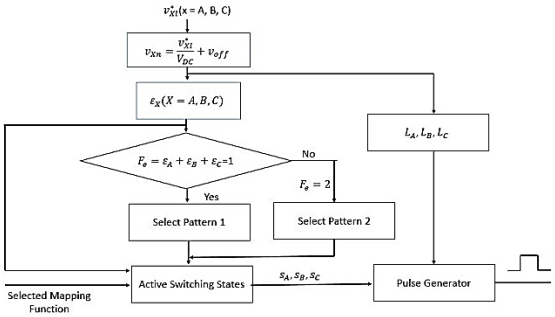


Figure 3. *Block diagram of the complete CMV elimination PWM method [5].*

3. SPIKES REDUCTION FOR COMPLETE CMV ELIMINATION PWM METHOD.

3.1 Impact of Deadtime on CMV Waveform.

The spikes in common mode voltage can be reduced by taking the deadtime effect into account. The deadtime which is required to avoid shoot-through is the one of the reason the spikes exist in common mode voltage waveform.

The effect of the deadtime on the common mode voltage can be best illustrated by an example shown in Figure 4, 5, 6.

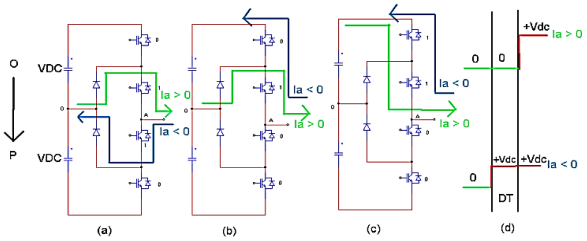


Figure 4. *Phase leg during O → P transition: (a) steady state V_{AO} = 0, (b) during dead time, (c) steady state V_{AO} = $+V_{DC}$, (d) pole voltage waveform with different current directions (I_{out} > 0: green, I_{out} < 0: blue) [6].*

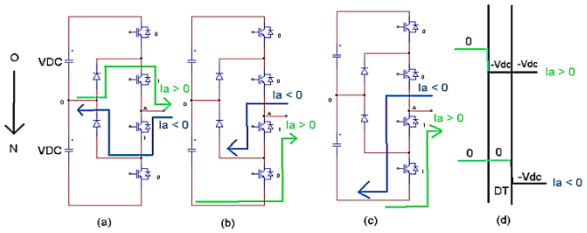


Figure 5. *Phase leg during O → N transition: (a) steady state V_{AO} = 0, (b) during dead time, (c) steady state V_{AO} = $-V_{DC}$, (d) pole voltage waveform with different current directions (I_{out} > 0: green, I_{out} < 0: blue) [6].*

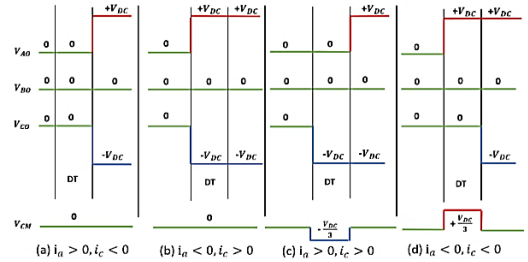


Figure 6. *Impact of Dead time on CM voltage generation [6].*

Fig. 4 represents the phase leg A during the transition from O to P state for two different phase current directions, i.e. $i_a > 0$ and $i_a < 0$. In this paper, the positive current $i > 0$ is defined as the one flowing towards the load while the negative one $i < 0$ is the one flowing away from the load or towards the inverter. In O state (SW_{1A} = 0, SW_{2A} = 1, SW_{3A} = 1, SW_{4A} = 0) as shown in Fig. 4(a), the pole voltage V_{AO} is equal to 0 as represented in Fig. 4(d) regardless of the phase current direction. However, during the deadtime interval (SW_{1A} = 0, SW_{2A} = 1, SW_{3A} = 0, SW_{4A} = 0) as shown in Fig. 4(b), the pole voltage V_{AO} depends on the phase current direction. If the current i_A is positive, it will be flowing from the neutral point, through the upper clamping diode and the switch SW_{2A}, then back to the load. Therefore, the pole voltage V_{AO} will be clamped to 0 as shown in Fig. 4(d). If the current i_a is negative, it will be flowing from the load towards the inverter, through the two free-wheeling diodes of the two switches SW_{1A} and SW_{2A}, then back to the positive rail of the upper DC-link voltage capacitor. Hence, the pole voltage V_{AO} will be equal to $+V_{DC}$ as shown in Fig. 4(d). Fig. 4(c) illustrates the phase leg A in P state (SW_{1A} = 1, SW_{2A} = 1, SW_{3A} = 0, SW_{4A} = 0). The pole voltage V_{AO} for which state will be $+V_{DC}$ as shown in Fig. 4(d) irrespective of the phase current direction. The same principle also applies to the phase leg B and C.

Fig. 5 demonstrates the phase leg A during the commutation from O to N state for two different phase current directions, i.e. $i_a > 0$ and $i_a < 0$. In O state (SW_{1A} = 0, SW_{2A} = 1, SW_{3A} = 1, SW_{4A} = 0) as shown in Fig. 5(a), the pole voltage V_{AO} will be equal to 0 as illustrated in Fig. 5(d) regardless of the phase current direction. However, during the deadtime period (SW_{1A} = 0, SW_{2A} = 0, SW_{3A} = 1, SW_{4A} = 0) as shown in Fig. 5(b), the pole voltage V_{AO} depends upon the phase current direction. If the current i_A is positive, it will be flowing from the negative rail of the

lower DC-link voltage capacitor, through the two free-wheeling diodes of the switches SW_{3A} and SW_{4A}, then towards the load. Hence, the pole voltage V_{AO} will be clamped to $-V_{DC}$ as shown in Fig. 5(d). On the other hands, if the current i_A is negative, it will be flowing from the load, towards the inverter, through the switch SW_{3A} and the lower clamping diode, then back to the neutral point. Therefore, the pole voltage V_{AO} will be 0 as shown in Fig. 5(d). Fig. 5(c) shows the phase leg A in N state (SW_{1A} = 0, SW_{2A} = 0, SW_{3A} = 1, SW_{4A} = 1). The pole voltage V_{AO} will be $-V_{DC}$ as shown in Fig. 5(d) irrespective of the phase current direction. The same principle also applies to the phase leg B and C.

With regard to the transition P→O and N→O, the rule is precisely the same as the transition shown in Fig. 4 and Fig. 5. Instead of transitioning from O→P and O→N as shown in Fig. 4 and 5, the transition of P→O and N→O will be repeated exactly the same in reverse. For example, as the phase leg A changes from O to P state with the deadtime, the pole voltage V_{AO} in O state, during the deadtime, and in P state will be equal to 0, 0, $+V_{DC}$, respectively for $i_A > 0$ and 0, $+V_{DC}$, $+V_{DC}$, respectively for $i_A < 0$. On the other hand, when the phase leg A transitions from P to O state with the deadtime, the pole voltage V_{AO} in P state, during the deadtime, and in O state will be $+V_{DC}$, 0, 0, respectively for $i_A > 0$ and $+V_{DC}$, $+V_{DC}$, 0, respectively for $i_A < 0$.

Fig. 6 demonstrates the common mode voltage generation during the deadtime interval for the transition from OOO to PON state of the three phase legs for 4 different phase current directions, i.e. $i_A > 0$ $i_C < 0$, $i_A < 0$ $i_C > 0$, $i_A > 0$ $i_C > 0$, $i_A < 0$, $i_C < 0$. In Fig. 6(a), the phase current directions of phase A and C are opposite, i.e. $i_A > 0$, $i_C < 0$. Since the phase leg A transitions from O to P state for the phase current $i_A > 0$, the pole voltage V_{AO} remains 0 during the deadtime period as explained in Fig. 4. Likewise, because the phase leg C changes from O to N state for the phase current $i_C < 0$, the pole voltage V_{CO} will be clamped to 0 during the deadtime period as described in Fig. 5. As for the phase leg B, the pole voltage V_{BO} remains 0 during the deadtime interval since there is no switching transition. Therefore, the common mode voltage will be $V_{CM} = \frac{V_{AO}+V_{BO}+V_{CO}}{3} = 0$ during the deadtime interval for the case in Fig. 6(a). Fig. 6(b) demonstrates the common mode voltage generation during the deadtime period, in which the phase current directions of phase A and C are opposite, i.e. $i_A < 0$, $i_C > 0$. Since the phase leg A changes from O to P state for the phase current $i_A < 0$, the pole voltage V_{AO} will be clamped to $+V_{DC}$ during the deadtime. Similarly, because the phase leg C transitions from O to N state for the phase current $i_C > 0$, the pole voltage V_{CO} will be $-V_{DC}$ during the deadtime. Finally, the pole voltage V_{BO} remains at 0 during the deadtime since there is no switching commutation. Hence, the common mode voltage will be $V_{CM} = \frac{V_{AO}+V_{BO}+V_{CO}}{3} = 0$ during the deadtime interval for the case $i_a < 0$, $i_C > 0$. Fig. 6(c) further shows the common mode voltage generation during the deadtime, in which the phase current direction of phase A and C are the same, i.e. $i_A > 0$, $i_C > 0$. The pole voltage V_{AO} is equal to 0 during the deadtime interval since there is a transition from O to P state for the phase current direction $i_A > 0$. Likewise, the pole voltage V_{CO} equals $-V_{DC}$ during the deadtime since there is a commutation from O to N state for the phase current $i_C > 0$. The pole voltage V_{BO} remains 0 during the deadtime since there is no switching transition. Therefore, the common mode voltage during the deadtime will be $V_{CM} = \frac{V_{AO}+V_{BO}+V_{CO}}{3} = \frac{0+0-V_{DC}}{3} = -\frac{V_{DC}}{3}$ for the case $i_A > 0$, $i_C > 0$. Fig. 6(d) illustrates the common mode voltage generation during the deadtime interval for the case $i_A < 0$, $i_C < 0$. The pole voltage V_{AO} will be equal to $+V_{DC}$ during the deadtime since there is a

transition from O to P state for the phase current direction $i_A < 0$. Likewise, the pole voltage V_{CO} will be 0 since there is a commutation from O to N state for the phase current direction $i_C < 0$. Similarly, the pole voltage V_{BO} remains 0 during the deadtime since there is no switching commutation. Hence, the common mode voltage during the deadtime interval will be $V_{CM} = \frac{V_{AO}+V_{BO}+V_{CO}}{3} = \frac{+V_{DC}+0+0}{3} = +\frac{V_{DC}}{3}$. The V_{DC} value mentioned in this section refers to the voltage on each DC-link capacitor assuming that the voltages of two DC-link capacitors are balanced. Generally, in order for the common mode voltage theoretically remains 0 during the deadtime interval, there must be simultaneous commutations of the two phase legs of which the phase current directions are opposite. If there are simultaneous commutations of the two phase legs whose the phase current directions are the same, the common mode voltage no longer remains zero during the deadtime. Based on this analysis, the complete CMV elimination pulse-width modulation strategy with spike reduction is proposed.

3.2 Proposed PWM Method for Complete CMV Elimination with Spike Reduction.

The proposed PWM strategy for complete CMV elimination with spike reduction is based on the impact of deadtime on CMV waveform as explained in Section 3.1.

There are six possible mapping functions available as shown in Table 1 and the control purpose which is to reduce the common mode voltage spikes will determine which phase maps into which sequence. In order to reduce spike in CMV waveform, the simultaneous commutations of any two-phase legs of which current directions are opposite must be guaranteed. Therefore, the control purpose in this paper is to map any two-phase legs having opposite current directions to any two sequences having simultaneous commutations.

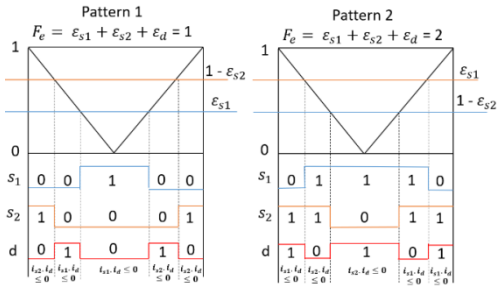


Figure 7. *Current direction condition shown at the bottom of the two patterns to theoretically eliminate CMV spikes [5].*

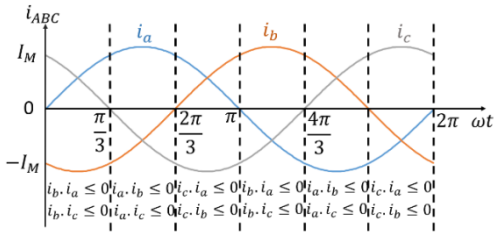


Figure 8. *The signs of the three-phase current in a fundamental period.*

The condition of the two particular phase currents is shown at the bottom of Fig. 7 for both switching patterns 1 and 2 to theoretically eliminate the common mode voltage spikes during the deadtime interval. For the sake of brevity, only the first half of the switching period in pattern 1 will be explained since the switching sequence is repeated in reverse in the second half of switching period and the pattern 2 is precisely the same as the pattern 1. As far as the pattern 1 is concerned, the two-level switching sequence of [s_1, s_2, d] in the first half of the switching period is 010→001→100. From 010 to 001, there are simultaneous commutations in s_2 and d sequences. Therefore, the current condition of these two sequences must be $i_{s2}.i_d \le 0$ in order for the common mode voltage to be zero during the deadtime interval. From 001 to 100, there are simultaneous transitions of s_1 and d sequences. Hence, the current condition of these two sequences must be $i_{s1}.i_d \le 0$. Over one switching period of both pattern 1 and 2 as shown in Fig. 7, the sign of the d-sequence current is always opposite to that of either s_1-sequence or s_2-sequence current. Moreover, since the frequency of the carrier is much larger than that of the three-

phase currents ($f_{carrier}$ = 5 KHz, f_0 = 50 Hz), the signs of the three-phase currents can be assumed to be constant during a sampling period. As shown in Fig. 8, there are six regions in which the sign of a particular phase current will be opposite to that of the other two-phase currents. In other words, the multiplication of one particular phase current with the other two-phase ones will be negative. For example, in Fig. 8, the phase-B current direction is opposite to both of those of phase-A and phase-C currents from 0 to $\frac{\pi}{3}$ interval. Hence, phase B will be mapped to d-sequence while phase A and C will be arbitrarily mapped to s_1 and s_2 sequences for $[0, \frac{\pi}{3}]$ interval. In other words, the task of reducing spikes in CMV waveform is to map one particular phase whose current has the opposite sign with respect to that of the other 2 phases to d-sequence. The other two phases will be mapped arbitrarily to either s_1 or s_2 because it does not have any impact on the CMV pulse during the deadtime.

The selected mapping function can be expressed in pseudo-code as follows:

If ($i_b.i_a \leq 0$ && $i_b.i_c \leq 0$)
  Phase b → d sequence
  Phase a → s_1 sequence
  Phase c → s_2 sequence
Else if ($i_a.i_b \leq 0$ && $i_a.i_c \leq 0$)
  Phase a → d sequence
  Phase b → s_1 sequence
  Phase c → s_2 sequence
Else if ($i_c.i_a \leq 0$ && $i_c.i_b \leq 0$)
  Phase c → d sequence
  Phase a → s_1 sequence
  Phase b → s_2 sequence

4. SIMULATION AND EXPERIMENTAL RESULTS

4.1 Simulation Results

The simulation results are obtained from MATLAB Simulink for the three-level neutral point clamped inverter under the condition of V_{DC} = 200 V, f_0 = 50 Hz, $f_{carrier}$ = 5 KHz, C_1 = C_2 = 4700 μF, R_a = R_b = R_c = 33.3 Ω, L_a = L_b = L_c = 2.7 mH. In Fig. 9, the comparison in terms of the total harmonics distortion of line-line voltage is made among three PWM strategies, i.e. Proposed Zero CMV PWM with reduced spikes, Zero CMV PWM with reduced current ripple [4], and Conventional Sinusoidal PWM. As expected, the total harmonic distortion of line-line voltage in the Conventional Sinusoidal PWM is significantly lower than those of the Proposed Zero CMV PWM with reduced spikes and Zero CMV PWM with reduced current ripple [4]. This is due to the fact that the Conventional Sinusoidal PWM utilizes the three nearest vectors to synthesize the reference vector while the other two methods employ the three farther zero common mode vectors. In terms of the two Zero CMV PWM methods, the Zero CMV PWM with reduced current ripple [4] has lower THD values of line-line voltage than those of the Proposed Zero CMV PWM with reduced spikes. It is expected since the aim of the Zero CMV PWM with reduced current ripple is to select the mapping functions as shown in Table 1 to minimize the output current ripple [4], which consequently lowers the total harmonic distortion of line-line voltage. The total harmonic distortion is calculated up to 200th harmonic of the fundamental frequency (f_0 = 50Hz).

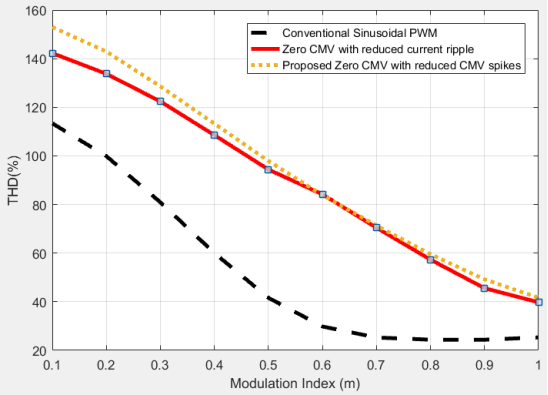
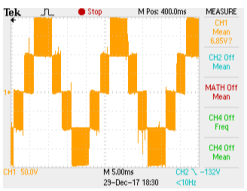


Figure 9. *The total harmonic distortion of line-line voltage with respect to modulation index for R_a = R_b = R_c = 33.3 Ω, L_a = L_b = L_c = 2.7 mH, V_{DC} = 200V, f_0 = 50 Hz, $f_{carrier}$ = 5 KHz.*

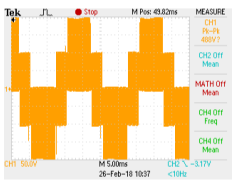
4.2 Experimental Results

In order to demonstrate the effectiveness of the proposed method, the experiment is conducted for the three-level NPC inverter. The DC-link voltage is held at 200V. The two DC-link capacitors C_1 and C_2 have a capacitance value of 4700 μF. The selected fundamental frequency f_0 is 50 Hz while the carrier frequency $f_{carrier}$ is 5 KHz. The three-phase balanced R-L load is $R_a = R_b = R_c = 33.3\ \Omega$, $L_a = L_b = L_c = 2.7$ mH and the deadtime is set to $2\mu s$. The modulation index m is 0.8 in the experiment. In an online spike reduction algorithm, the two Hall current sensors are used to calculate the signs of the three-phase currents. Since the three-phase load is balanced, the third current can be derived from the other two ones.

The waveforms of line-line voltage output are shown in Fig. 10(a) for the Conventional Sinusoidal PWM method and in Fig. 10(b) for the Proposed Zero CMV PWM strategy with spike reduction. The total harmonics distortion (THD) of line-line voltage output in the Conventional Sinusoidal PWM method is 28.4% as opposed to 68.1% in the proposed Zero CMV PWM strategy. The THD of the proposed method is higher than that of the conventional sinusoidal PWM strategy is due to the fact that the conventional sinusoidal PWM method utilizes the three nearest vectors to synthesize the reference vector, thereby achieving the optimal harmonics performance while the reference vector in the proposed method is synthesized by three farther zero common mode vectors. The THD in the experiment is calculated up to 200th harmonic of the fundamental frequency (f_0 = 50 Hz).

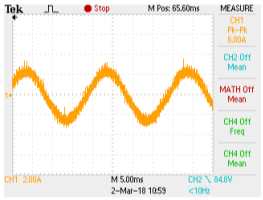


(a) Conventional sinusoidal PWM method (THD = 28.4%).

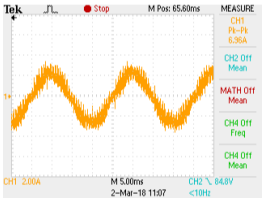


(b) Zero Common mode voltage PWM method with spike reduction (THD = 68.1%).

Figure 10. *Waveforms of line-line voltage V_{AB} at modulation index m = 0.8, f_0 = 50 Hz, $f_{carrier}$ = 5 KHz, $R_a = R_b = R_c = 33.3\ \Omega$, $L_a = L_b = L_c = 2.7$ mH, $C_1 = C_2 = 4700\ \mu F$, X-axis: 5ms/div, Y-axis: 50V/div.*



(a) Conventional sinusoidal PWM method (THD = 7.48%).



(b) Zero Common mode voltage PWM method with spike reduction (THD = 19.92%).

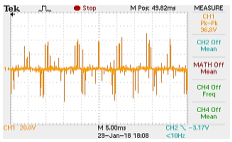
Figure 11. *Waveforms of phase current output at modulation index m = 0.8, V_{DC} = 200V, f_0 = 50 Hz, $f_{carrier}$ = 5 KHz, $R_a = R_b = R_c = 33.3\ \Omega$, $L_a = L_b = L_c = 2.7$ mH, X-axis: 5ms/div, Y-axis: 2A/div.*

The waveforms of output phase current in the conventional sinusoidal PWM and the proposed Zero CMV PWM with spike reduction are shown in Fig. 11(a) and Fig. 11(b), respectively. The THD of the phase current output in the conventional sinusoidal PWM is 7.48% while it is 19.92% in the proposed method. As expected, the THD of the phase current output in the sinusoidal PWM is lower than that of the proposed strategy for the same reason explained earlier.

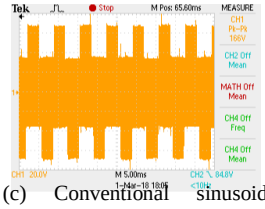
The waveforms of the common mode voltage for the proposed Zero CMV PWM with spike reduction, the Zero CMV PWM with reduced current ripple [4], and the conventional sinusoidal PWM are shown in Fig. 12(a), Fig. 12(b), and Fig. 12(c), respectively. As shown in Fig. 12(c), the common mode voltage has a peak value of 66.67V or one-third of the DC-link voltage input (V_{DC} = 200V) for the conventional sinusoidal PWM. As for the Zero CMV PWM with reduced current ripple [4] as shown in Fig. 12(b), the common mode voltage is virtually eliminated despite some spikes existing in the waveform partly due to the deadtime interval required in the real-world switching condition. Therefore, the spikes can be reduced by taking the

deadtime effect into account. In order to demonstrate the effectiveness of the proposed method, the frequency spectra of the three methods, i.e. the Conventional Sinusoidal PWM, the Zero CMV PWM with reduced current ripple [4], and the proposed CMV PWM with spike reduction are shown in Fig. 13 (a), (b), (c), respectively. The frequency spectra are analyzed up to 400th harmonic of the fundamental frequency (f_0 = 50 Hz). As shown in Fig. 13(a) for the frequency spectrum of the Conventional sinusoidal PWM method, the common mode voltage has a peak value of almost 50 V at switching frequency (5KHz), and of more than 10 V at 10 KHz. With regard to the frequency spectrum of Zero CMV PWM with reduced current ripple [4] as represented in Fig. 13(b), the peak value of common mode voltage is less than 0.8V at switching frequency and less than 1.2V at 10 KHz. The frequency spectrum of the proposed Zero CMV PWM with reduced spikes as shown in Fig. 13(c) is further improved, in which the peak values of the common mode voltage at all harmonics are less than 0.8V. Therefore, it demonstrates the effectiveness of the proposed strategy.

(a) Proposed Zero Common mode voltage PWM method with spike reduction.

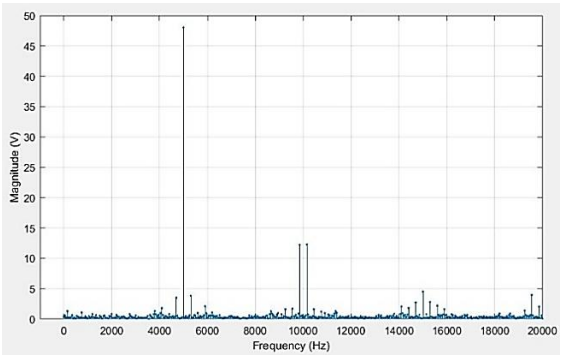


(b) Zero Common mode voltage PWM method with reduced current ripple [4].

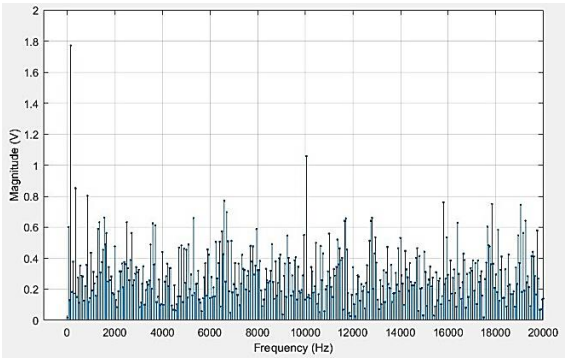


(c) Conventional sinusoidal PWM method.

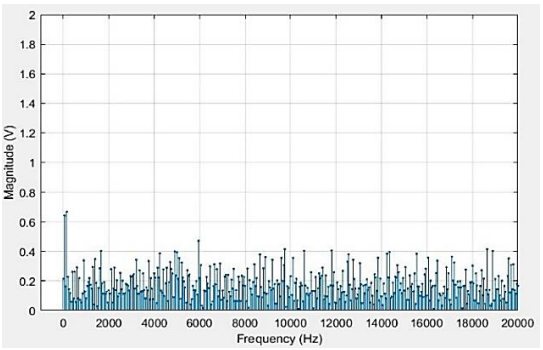
Figure 12. *Waveforms of the Common mode voltage at modulation index m = 0.8, f_0 = 50 Hz, R_a = R_b = R_c = 33.3 Ω, L_a = L_b = L_c = 2.7 mH, V_{DC} = 200 V, Y-axis: 20V/div, X-axis: 5.00ms/div.*



(a) Conventional sinusoidal PWM method.



(b) Zero Common mode voltage with reduced current ripple [4].



(c) Proposed Zero Common mode voltage with spike reduction.

Figure 13. *Frequency Spectra of the Common mode voltage at modulation index m = 0.8, V_{DC} = 200 V, f_0 = 50 Hz, $f_{carrier}$ = 5 KHz, R_a = R_b = R_c = 33.3 Ω, L_a = L_b = L_c = 2.7 mH, deadtime = 2μs.*

5. CONCLUSION

This paper proposes the PWM strategy to eliminate the common mode voltage for the three-level neutral point clamped inverter by utilizing the principle of three zero common mode voltage vectors. The modulation process of the three-level NPC inverter is simplified to that of the two-level

inverter. The two standardized virtual PWM patterns are then proposed to cover the whole space vector diagram. There are six possible mapping functions corresponding to each PWM pattern and selecting which mapping function depends upon the control purpose. The deadtime effect is investigated thoroughly and the PWM method with spike reduction is proposed based on the deadtime analysis. Experimental results confirm the effectiveness of the proposed strategy in eliminating the common mode voltage and reducing its spikes.

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