Journal of Technical Education Science No.42 (6/2017)
Ho Chi Minh City University of Technology and Education

SOME NEW RESULTS IN SIMULATION OF SINGLE ELECTRON TRANSITOR

MỘT SỐ KẾT QUẢ MỚI TRONG MÔ PHỎNG TRANSISTOR ĐƠN ĐIỆN TỬ

Le Hoang Minh[1], Dinh Sy Hien[2]
[1]*Ho Chi Minh City University of Technology and Education, Vietnam*
[2]*The University of Science, VNU-HCM, Vietnam*

Received 16/01/2017, Peer reviewed 18/2/2017, Accepted for publication 25/2/2017

ABSTRACT

Single electron transistor (SET) is a key element in current research area of nano-electronics and nano-technology, which can offer nano-feature size, low power consumption, high operating speed and high-density integration. SET is a new nano-scale switching device; it can control the motion of the single electron and its operation is based on the tunneling effect. Research on SET by experiments is a challenge for researchers in current domestic conditions. Meanwhile, simulation is a research method which can achieve reliable results and feasible. Simulated results can be used to orient for manufacture and experiment. The goal of this work is to discuss briefly about physics of the SET and focuses on simulation of basic quantum device characteristics like tunneling effect, Coulomb blockage, Quantum dot, Coulomb staircase, and Coulomb oscillation. The current-voltage characteristics of SET are explored for illustration. Model of SETs based on one-energy level (metallic) and multi-energy level (semiconducting) has been proposed. Two types of metallic and semiconducting SETs have been simulated.

Keywords: *single electron transistor; current-voltage characteristics; Coulomb blockage; Coulomb staircase; Coulomb oscillation.*

TÓM TẮT

Transistor đơn điện tử (SET) là một yếu tố cơ bản trong lĩnh vực nghiên cứu về điện tử nano và công nghệ nano hiện nay. SET cho kích thước đặc tính nano, tiêu tốn công suất thấp, tốc độ làm việc cao và mật độ tích hợp cao. SET là một linh kiện chuyển mạch thang nano mới; có thể điều khiển chuyển động của một điện tử và hoạt động dựa trên hiệu ứng xuyên hầm. Việc nghiên cứu SET thực nghiệm trong nước chưa thể thực hiện được trong điều kiện hiện nay.Trong khi đó mô phỏng là phương pháp nghiên cứu cho ra kết quả đáng tin cậy và hoàn toàn thực hiện được. Kết quả mô phỏng sẽ định hướng cho chế tạo và thực nghiệm. Mục tiêu của bài báo này là bàn về vật lý của SET và tập trung lên mô phỏng đặc trưng lượng tử cơ bản của linh kiện như hiệu ứng xuyên hầm, khóa Coulomb, chấm lượng tử, bậc thang Coulomb và dao động Coulomb. Những đặc trưng dòng-thế được nghiên cứu kỹ dùng để minh họa. Mô hình của SET dựa trên một mức năng lượng (SET kim loại) và nhiều mức (SET bán dẫn). Hai loại SET kim loại và bán dẫn đã được mô phỏng.

Từ khóa: *Transistor đơn điện tử; đặc trưng dòng-thế; khóa Coulomb; bậc thang Coulomb; dao động Coulomb.*

1. INTRODUCTION

Rapid progress in microelectronics has pushed the MOSFET dimension toward the physical limit (10nm). In the future it is probable that the nano-MOSFETs could be replaced by new fundamental devices like single electron transistor (SET). SETs have attracted much attention for IC applications because of their nano-feature size, ultra-low power dissipation, high frequency, new functionalities, and CMOS compatible fabrication process [1].

After their discovery in the 1986 [2,3], there has been extensive research on fabrication, design and modeling of SETs [4]. SETs with a variety of structures were proposed and fabricated by using different methods [5-7]. SETs have been fabricated to operate at room temperature [8-10]. Molecular quantum dot [11] can display SET's behavior. 1D-structures, such as carbon nanotubes and nanowires, can act as SETs [7]. Recent advances in grapheme [12] show promise for SETs.

Research on SET modeling and simulation has been an active area. Monte Carlo simulation has been widely used to model SETs. SIMON [13] and MOSES [14] are the two most popular SET simulators. Uchida et al. proposed an analytical SET model and incorporated it into SPICE [15]. Inokawa et al. extended this model to a more general form to include asymmetric SETs [16]. Mahapatra et al. proposed a simulation framework for hybrid SET/CMOS circuit design and analysis [17]. In contrast, model used non-equilibrium Green's function method (NEGF) [18] commonly used in the nanoscale devices and are superior in terms of simplicity.

In this work, the physical properties of SET will be introduced and current-voltage characteristics in single electron transistor is simulated by non-equilibrium Green's function method using graphic user interface (GUI) of Matlab. Here, the authors propose a model of one-level for metallic SET and multiple-level for semiconducting SET. Also, summarization on the theoretical approach based on NEGF, review the capabilities of the simulator, NEMO-VN2 is done[19] to give examples of typical simulations of SET's current-voltage characteristics and compare simulated results with experimental ones.

2. PHYSICS, MODELING AND SIMULATION OF SINGLE ELECTRON TRANSISTOR

Basic physical properties of single electron transistor

The operation of a single electron tunneling device is governed by the Coulomb charging effect. As shown in Fig.1a, a single electron tunneling device consists of a nanometer-scale conductive (or semiconducting) island embedded in an insulating material. Electrons travel between the island, source (S) and drain (D) through thin insulating tunnel junctions. When an electron tunnels into the island, the overall electrostatic potential of the island increases by e/C_Σ, where e is the elementary charge and C_Σ is island capacitance. For large devices, this change in potential is negligible due to the high capacitance C_Σ. However, for nanometer-scale islands, C_Σ is much smaller (about aF).

Change to SET island potential results an energy gap at the Fermi energy, preventing further electron tunneling. This phenomenon is called Coulomb blockade. It prevents current from flowing between source and drain (I_{ds} = 0), i.e, the SET is turned off. The Coulomb blockade effect can be overcome by changing the voltage of a conductor gate capacitively coupled to the island, thereby turning tunneling on or off.

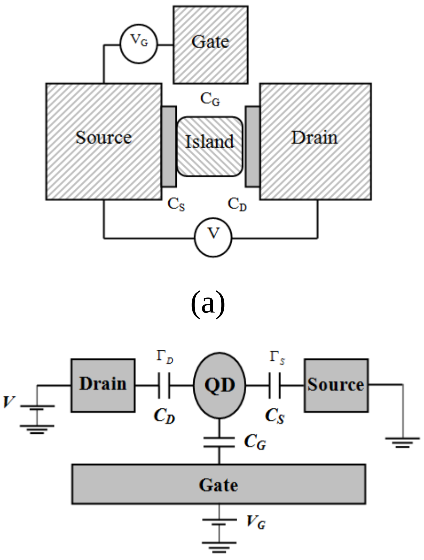
As shown in Fig.1 a SET typically has three terminals. The source and drain terminals serve as electron reservoirs. When the SET is turned on, electrons tunnel from one terminal, through the junction, to the conductive island. They then tunnel through the other junction to the other terminal. Each tunneling junction is modeled as resistor (R_S or R_D) and capacitor (C_S or C_D) in parallel.

A gate terminal (G), with coupling capacitance C_G, controls the transport of electrons. The Coulomb blockade effect is maximized when $V_{GS} = me/C_G$, where $m = \pm1, \pm2, \pm3, \cdots$ because, at these voltages, the system is in minimum-energy state when an integer number of electrons are present on the island. The Coulomb blockade effect vanishes when it is equal to $\pm 1/2, \pm 3/2, \cdots$, i.e., when m is a half-integer value because, at these voltages, the system is in a minimum-energy state when a half-integer number of electrons are present on the island. In this case, the single tunneling event does not move the system from a minimum energy state. Electrons can therefore tunnel, in single-file, through the island as determined by V_{DS}.

In order to observe the Coulomb blockade effect, the following constraints must be satisfied.

1) Since thermal fluctuations can suppress the Coulomb blockade effect, the electrostatic charging energy, e^2/C_Σ, must be much greater than k_BT, where k_B is Boltzmann's constant and T is the temperature. In order to ensure reliability, $e^2/C_\Sigma \geq k_B T$ other more conservative, $e^2/C_\Sigma \geq 40k_B T$ constraint is enforced. These equations imply that the maximum allowed island capacitance is inversely proportioned to temperature. At room temperature, an island capacitance below 1 aF is required. Island capacitance is function of island size. As shown in Table 1 room temperature operation requires an island size in the nanometer range, making fabrication challenging. At present, the smallest island capacitance of a fabricated device is around 0.15 aF [9].

2) To observe single-electron charging effects, electrons must be confined to the island, which requires that the junction resistance be higher the quantum resistance, i.e., R_S, $R_D > h/e^2$, $h/e^2 = 25.8\ \text{k}\Omega$, where h is Plank's constant. Therefore, SETs have high resistances and low driving current.



(a)

(b)

Figure 1.*(a) Structure of SET, (b) equivalent schematic diagram of SET: C_G - gate capacitance, C_S - source tunnel junction capacitance, C_D – drain tunnel junction capacitance, R_S – source tunnel junction resistance, R_D – drain tunnel junction resistance.*

So far methods of fabrication of single electron transistors can be divided into two categories: metallic and semiconducting SETs. Model of SETs based on energy band theory is shown in Figure 2 [18]. Depending on material of quantum dots, SETs can be grouped in two types: one-energy level (metallic) and multi-energy levels (semiconducting). In the case of multi-levels, distance between energy levels (ΔE) in quantum dot isinversely proportional to size of quantum dot.

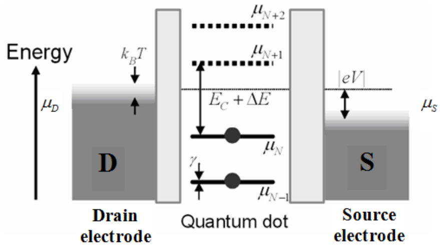


***Figure 2.** Model of single electron based on energy band theory.*

Simulation method and results

From point of view of fabrication methods, single electron transistors can be divided into two categories: SET with metallic island (namely metallic SET) and semiconducting island (namely semiconducting SET). SET's models can be also grouped in one level device and multi-level device respectively.

The flow of current is due to the difference in potentials between the source and the drain, each of which is in a state of local equilibrium, but maintained at different electro-chemical potentials $\mu_{1,2}$ and hence with two distinct Fermi functions:

$$f_1(E) = \frac{1}{exp\left[{(E-\mu_1)}/{k_BT}\right]+1} \qquad (1)$$

$$f_2(E) = \frac{1}{exp\left[{(E-\mu_2)}/{k_BT}\right]+1} \qquad (2)$$

by the applied bias V: $\mu_2 - \mu_1 = -qV$.

We describe a SET's model for metallic SET using one-level device. We describe a SET's model for a multiple-level device (semiconducting SET) whose energy levels are described by a Hamiltonian matrix [H] and whose coupling to the source and the drain contacts is described by self-energy matrices $[\Sigma_1(E)]$ and $[\Sigma_2(E)]$respectively (Fig.3).

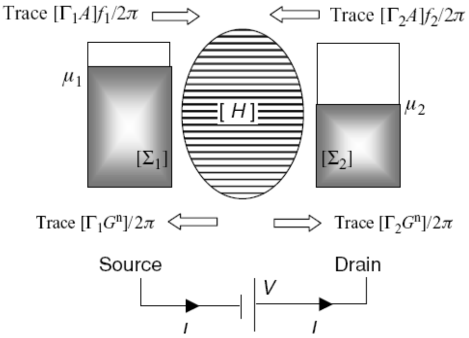


Figure 3. Multi-level device whose energy levels are described by a Hamiltonian matrix [H] and whose coupling to the source and drain contacts is described by self-energy matrices $[\Sigma_1(E)]$ and $[\Sigma_2(E)]$ respectively.

Here, E- energy, k_B - Boltzmann constant, T- temperature.

The density matrix is given by

$$\rho = \int_{-\infty}^{+\infty} \frac{dE}{2\pi} G^n(E) = \int_{-\infty}^{+\infty} \frac{dE}{2\pi} [A_1(E) f_1(E) + A_2(E) f_2(E)] \qquad (3)$$

The current I_D flows in the external circuit is given by Landauer formula [18]:

$$I_D = (q/h) \int_{-\infty}^{+\infty} dE T(E) j(f_1(E) - f_2(E)) \qquad (4)$$

The quantity T(E) appearing in the current equation (4) is called the transmission function, which tells us the rate at which electrons transmit from the source to the drain contacts by propagating through the device. Knowing the device Hamiltonian [H] and its coupling to the contacts described by the self-energy matrices $\Sigma_{1,2}$, we can calculate the current from (4). For coherent transport, one can calculate the transmission from the Green's function method, using the relation:

$$T(E) = Trace[\Gamma_1 G \Gamma_2 G^+] + Trace[\Gamma_2 G \Gamma_1 G^+] \quad (5)$$

The appropriate NEGF equations are obtained:

$$G = [EI - H - \Sigma_1 - \Sigma_2]^{-1}, \Gamma_{1,2}$$

$$= i[\Sigma_{1,2} - \Sigma_{1,2}^+], A_1(E) = GI,$$

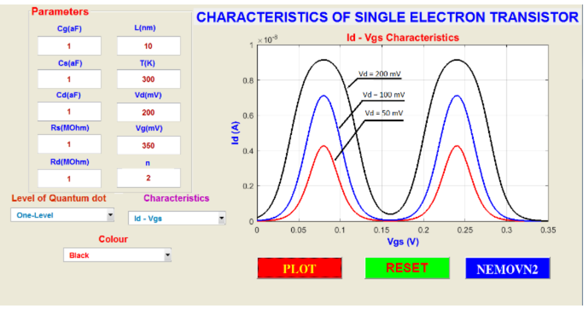
$$G^n = [A_1]f(E) + [A_2]f(E), \quad ($$

$$A = i[G - G^+] = [A_1] + [A_2] \quad 6)$$

Where H is effective mass Hamiltonian, I is an identity matrix of the same size, $\Gamma_{1,2}$ are the broadening functions, $A_{1,2}$ are partial spectral functions, A(E) are spectral function, G^n is correlation function. We use a discrete lattice with N points spaced by lattice spacing "a" to calculate the eigen-energies for electrons in the quantum dot.

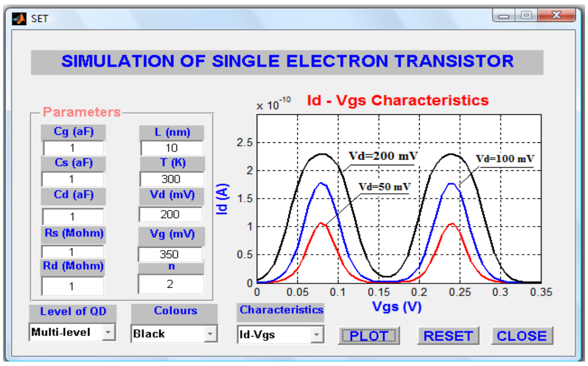
By utilizing the simulator namely NEMO-VN2 [19], the I_D–V_G characteristics of SET having the given parameters are shown in Fig.3.

Fig.4 demonstrates the typical Coulomb oscillation behavior in SET I_D-V_G characteristics. It shows that the SET Coulomb oscillation period (e/C_G, e is the electronic charge) is dictated by SET's gate capacitance. Values of gate voltage at the first and the second peaks are $e/2C_G$ (80 mV) and $3e/2C_G$ (240 mV) respectively. Here, it should be emphasized that the peak and the valley currents of Coulomb oscillations are perfectly represented by the model. The results calculated according to model ($e/2C_G$ for C_G = 1 aF) coincide well with the simulated ones. Current-voltage (I_D-V_G) characteristics showing the suppression of the Coulomb oscillation by broadening current peaks increased at high V_D (200 mV). It also reveals the fact that it is difficult to obtain the Coulomb oscillations in the device characteristics at high V_D greater than $3e/C_T$ (C_T is total capacitance of SET), (160 mV). It should note that high drain voltage, V_D undermines SET's current-voltage characteristics. Characteristics of metallic and semiconducting SET shown in Figure 4a and 4b respectively.



Cg(aF) 1
L(nm) 10
Cs(aF) 1
T(K) 300
Cd(aF) 1
Vd(mV) 200
Rs(MOhm) 1
Vg(mV) 350
Rd(MOhm) 1
n 2
Level of Quantum dot: One-Level
Characteristics: Id - Vgs
Colour: Black

(a)



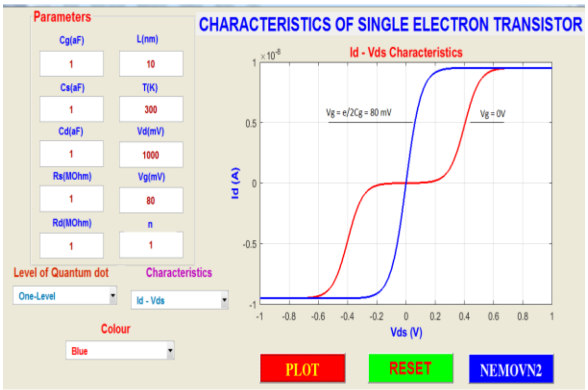
Cg (aF) 1
L (nm) 10
Cs (aF) 1
T (K) 300
Cd (aF) 1
Vd (mV) 200
Rs (Mohm) 1
Vg (mV) 350
Rd (Mohm) 1
n 2
Level of QD: Multi-level
Colours: Black
Characteristics: Id-Vgs

(b)

Figure 4. *Typical I_D-V_G characteristics (Coulomb oscillations) of SET simulated by the simulator NEMO-VN2 for various values of V_D = 50 mV, 100 mV and 200 mV at room temperature, T = 300K. The SET parameters are: L = 10 nm, $C_G = C_S = C_D$ = 1aF and $R_S = R_D$ = 1 MΩ: a) one level SET, b) Multi-level SET*

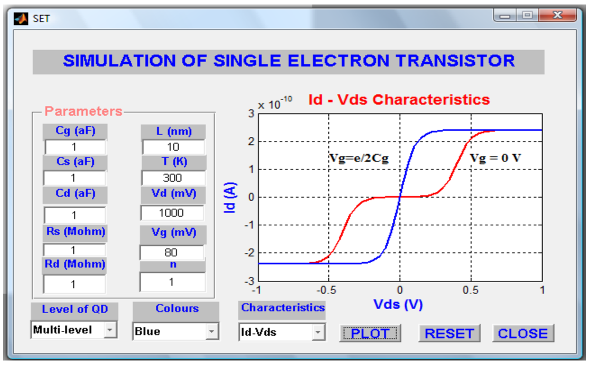
Fig.5 reproduces SET's I_D-V_D characteristics at room temperature (T = 300K) for different gate biases, V_G = 0 mV and $V_G = e/2C_G$ (Coulomb oscillation). Characteristics of metallic and semiconducting SET shown in Figure 5a and 5b respectively.

For V_G = 0 mV, V_D starts from the Coulomb blockade region and increases (or decreases) through the single-electron tunneling region. For $V_G = e/2C_G$ (at the first Coulomb oscillation peak), I_D starts from zero and increases (or decreases) linearly. The threshold voltage of SET is $V_G = e/2C_G$.



Cg(aF) 1
L(nm) 10
Cs(aF) 1
T(K) 300
Cd(aF) 1
Vd(mV) 1000
Rs(MOhm) 1
Vg(mV) 80
Rd(MOhm) 1
n 1
Level of Quantum dot: One-Level
Characteristics: Id - Vds
Colour: Blue

(a)



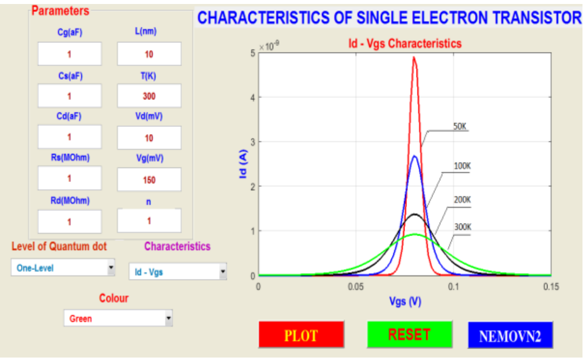
Cg (aF) 1
L (nm) 10
Cs (aF) 1
T (K) 300
Cd (aF) 1
Vd (mV) 1000
Rs (Mohm) 1
Vg (mV) 80
Rd (Mohm) 1
n 1
Level of QD: Multi-level
Colours: Blue
Characteristics: Id-Vds

(b)

Figure 5. *I_D-V_D characteristics simulated by the simulator at room temperature T = 300K for various values of V_G = 0 mV and $V_G = e/2C_G$. The SET parameters are: L = 10 nm, $C_G = C_S = C_D$ = 1 aF and $R_S = R_D$ = 1 MΩ: a) One-level SET, b) Multi-level SET.*

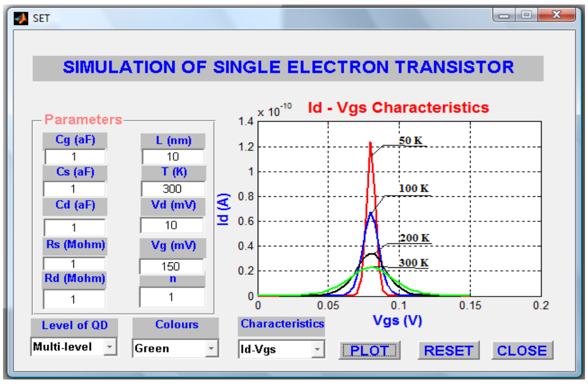
Figure 6 represents I_D-V_G characteristics with the value of V_D = 10 mV at different temperatures. One can note that the effects of temperature on Coulomb oscillations are strongly. The Coulomb oscillations of SET are clear at low temperature (at 50K). Current-voltage (I_{DS}-V_G) characteristics showing the suppression of the Coulomb oscillation by broadening current peaks increased at higher temperature (100K, 200K, and 300K). It also reveals the fact that it is no more possible to obtain the Coulomb oscillations in the device characteristics at high temperature. It should note that high temperature undermines SET's current-voltage characteristics.

Characteristics of metallic and semiconducting SET shown in Figure 6a and 6b respectively.



Cg(aF) 1
L(nm) 10
Cs(aF) 1
T(K) 300
Cd(aF) 1
Vd(mV) 10
Rs(MOhm) 1
Vg(mV) 150
Rd(MOhm) 1
n 1
Level of Quantum dot: One-Level
Characteristics: Id - Vgs
Colour: Green

(a)

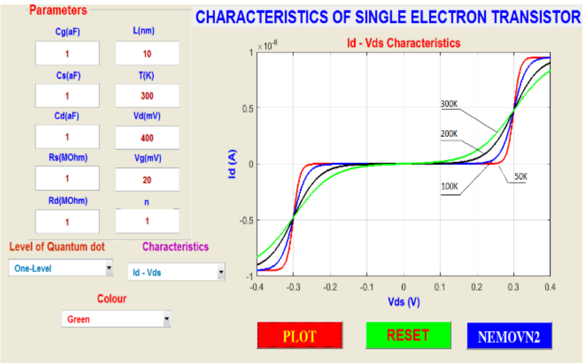


Cg (aF) 1
L (nm) 10
Cs (aF) 1
T (K) 300
Cd (aF) 1
Vd (mV) 10
Rs (Mohm) 1
Vg (mV) 150
Rd (Mohm) 1
n 1
Level of QD: Multi-level
Colours: Green
Characteristics: Id-Vgs

(b)

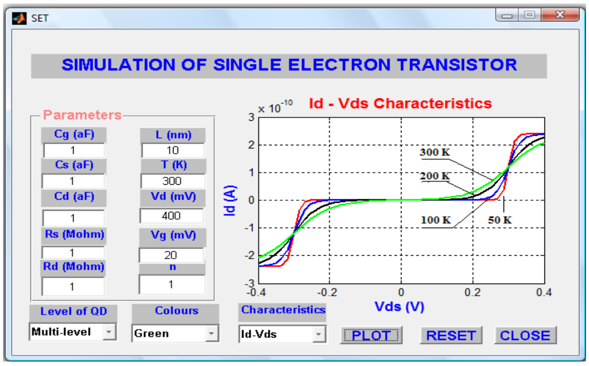
Figure 6. *Typical I_D-V_G characteristics simulated by the simulator for value of V_D = 10 mV at different temperatures: 50K, 100K, 200K, 300K. The SET device parameters are: L = 10 nm, $C_G = C_S = C_D$ = 1aF and $R_S = R_D$ = 1 MΩ: a) One-level, b) Multi-level.*

The effect of temperature (T) on the device characteristics is also demonstrated in figure 7, and it shows that the Coulomb blockade region becomes thinner at higher temperatures. Therefore, an accurate model for SET simulation must be to capture both the effect of temperature and the effect of high V_D on the device characteristics. Characteristics of metallic and semiconducting SET shown in Figure 7a and 7b respectively.



Cg(aF) 1
L(nm) 10
Cs(aF) 1
T(K) 300
Cd(aF) 1
Vd(mV) 400
Rs(MOhm) 1
Vg(mV) 20
Rd(MOhm) 1
n 1
Level of Quantum dot: One-Level
Characteristics: Id - Vds
Colour: Green

(a)



Cg (aF) 1
L (nm) 10
Cs (aF) 1
T (K) 300
Cd (aF) 1
Vd (mV) 400
Rs (Mohm) 1
Vg (mV) 20
Rd (Mohm) 1
n 1
Level of QD: Multi-level
Colours: Green
Characteristics: Id-Vds

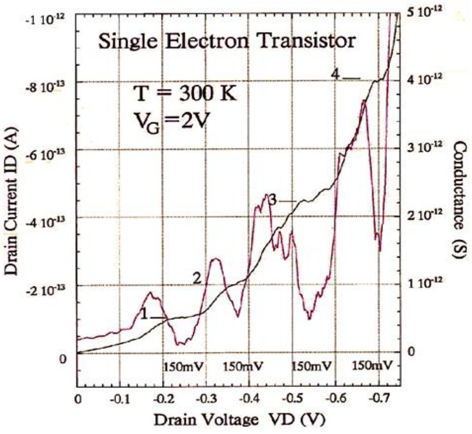
(b)

Figure 7. *Typical I_{DS}-V_{DS} characteristics simulated by the simulator for value of V_G = 20 mV at different temperatures (T): 50K, 100K, 200K, and 300K. The SET device parameters are: L = 10 nm, C_G = C_S = C_D = 1aF and R_S = R_D = 1 MΩ: a) One-level SET, b) Multi-level SET*

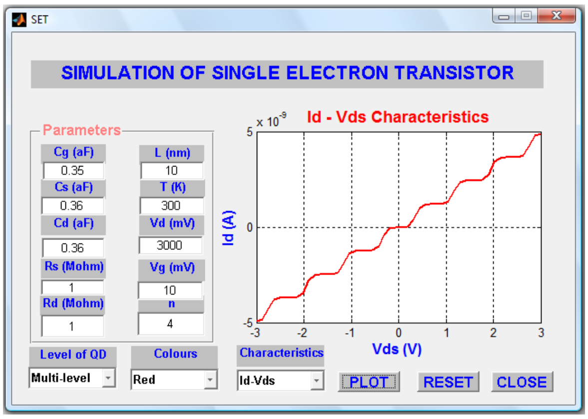
Accuracy of the model is evaluated by comparing simulated results with experimental ones from [8].

According to the work [8], its authors have succeeded in fabricating an SET. The SET operates at room temperature, showing a clear Coulomb staircase with a ~150 mV period at 300 K. The drain current-voltage characteristics of the SET were measured at room temperature and are shown in figure 8a. The gate bias was set to 2 V. In the Figure, the solid lines show the current of the SET, and the dashed line shows the conductance of the SET. Between the drain bias of 0 V and -0.75 V, four clear Coulomb staircases with a ~150 mV period are observed. The drain current versus gate bias characteristics with 150 mV drain bias at room temperature exhibit clear current oscillations with a period of ~460 mV, implying a periodic Coulomb oscillation of the current. Figure 8b,c reproduce I_D-V_D characteristics and conductance of the same SET having length, L = 10 nm at temperature of 300 K. Figures 8b,c show simulated results of I_D-V_D characteristics and conductance of the same SET.

Four clear Coulomb staircases are shown in simulated results on I_D-V_D characteristics (Figure 8b). Four clear conductance peaks are also shown in Figure 8c. The results simulated according to the model coincide well with the experimental ones at least in the same shape.

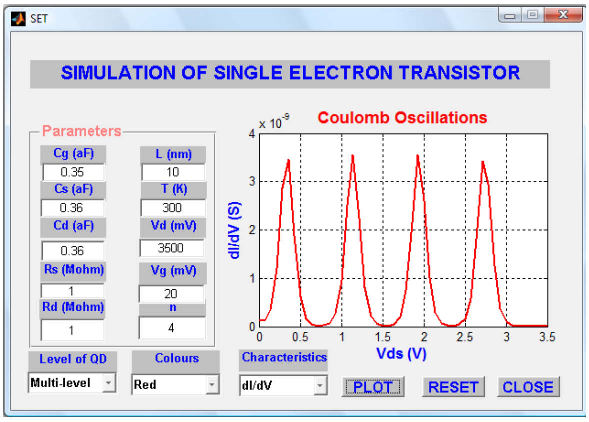


a)



Parameters
Cg (aF): 0.35
Cs (aF): 0.36
Cd (aF): 0.36
Rs (Mohm): 1
Rd (Mohm): 1
L (nm): 10
T (K): 300
Vd (mV): 3000
Vg (mV): 10
n: 4
Level of QD: Multi-level
Colours: Red
Characteristics: Id-Vds

(b)

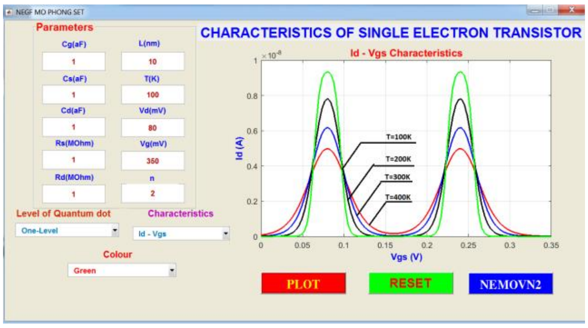


Parameters
Cg (aF): 0.35
Cs (aF): 0.36
Cd (aF): 0.36
Rs (Mohm): 1
Rd (Mohm): 1
L (nm): 10
T (K): 300
Vd (mV): 3500
Vg (mV): 20
n: 4
Level of QD: Multi-level
Colours: Red
Characteristics: dI/dV

(c)

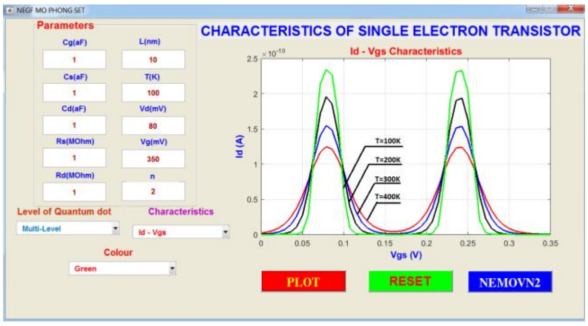
Figure 8. *a) Drain current versus drain voltage characteristics of the SET at 300 K [8]: V_D = 150 mV, C_t = 0.36 aF, C_G = 0.35 aF; b) I_D-V_D characteristics simulated; c) Conductance characteristics simulated by the simulator, NEMO-VN2 for value of V_G = 20 mV. The SET device parameters are: L = 10 nm, C_G = 0.35 aF, C_S = C_D = 0.36 aF and R_S = R_D = 1 MΩ.*

Affects of temperature on current-voltage characteristics of SET in two modes of operation have been also considered (Figure 9). Current-voltage characteristics (I_{DS}-V_{GS}) in two modes of operation have been dismissed while temperature increasing. Differences of current-amplitude in two modes of operation have been observed about 100 times.



Parameters
Cg(aF): 1
Cs(aF): 1
Cd(aF): 1
Rs(MOhm): 1
Rd(MOhm): 1
L(nm): 10
T(K): 100
Vd(mV): 80
Vg(mV): 350
n: 2
Level of Quantum dot: One-Level
Characteristics: Id - Vgs
Colour: Green

(a)



Parameters
Cg(aF): 1
Cs(aF): 1
Cd(aF): 1
Rs(MOhm): 1
Rd(MOhm): 1
L(nm): 10
T(K): 100
Vd(mV): 80
Vg(mV): 350
n: 2
Level of Quantum dot: Multi-Level
Characteristics: Id - Vgs
Colour: Green

(b)

Figure 9. *Typical I_{DS}-V_{GS} characteristics simulated by the simulator for value of V_{DS} = 80 mV at different temperatures (T): 100K, 200K, 300K, and 400K. The SET device parameters are: L = 10 nm, C_G = C_S = C_D = 1aF and R_S = R_D = 1 MΩ: a) One-level SET, b) Multi-level SET.*

3. CONCLUSIONS

Physical properties,fabrication methods, and the most popular simulators of SET have been introduced. A model for SET device using NEGF written in GUI of Matlab has been reported. We have proposed model for simulation of two types of SET: one-level mode for metallic SET and multi-level mode for semiconducting SET. The proposed model has been verified at one-level and multiple-level for SET's device. A set of simulations is then successfully performed for various parameters of the SET's device in one-level and multi-level mode. The model is not only able to accurately describe I_D-V_G,

I_D-V_D SET's characteristics, but also affects of gate materials, size of SET, temperature on SET's characteristics. Different SET's characteristics (I_D-V_G, I_D-V_D, effect of temperature) have been simulated. It has been found that currents in metallic SET were greater than in semiconducting SET about 100 times. The simulated results are also compared with experimental ones [8] and good agreements are validated.

REFERENCES

[1] International technology roadmap for semiconductors, (2006), http://public.itrs.net.

[2] D. V. Averin, K. K. Likharev, Coulomb blockade of tunneling and coherent oscillations in small tunnel junctions, *J. Low Temperature Physics*, 62,345-372 (1986).

[3] T. A. Fulton, J. G. Dolan, Observation of single electron charging effects in small tunnel junctions, *Physics Review Lett.*, 59, 109-112(1987).

[4] K.K. Likharev, Single electron devices and their applications, *Proc. IEEE*, 87, pp. 606-632, (1999).

[5] Y. Nakamura, C. D. Chen, J. S. Tsai, 100 K operation of Al-based single electron transistors, *Japan Journal of Applied Physics*, 35, 1465-1467(1996).

[6] X. Tang, X. Baie, V. Bayot, F. Van de Wiele, J. P. Colinge, An SOI single electron transistor, *Proceedings of Silicon on Insulator Conference*, Oct. 1999,46-47 (1999).

[7] M. Ahlskog, R Tarkiainen, L. Roschier, P. Hakonen, Single electron transistor made of two crossing multi-walled carbon nanotubes and its noise properties, *Applied Physics Lett.*, 77,4037-4039(2000).

[8] K. Matsumoto, M. Ishii, K Segawa, Y. Oka, B. J. Vartanian, J.S.Harris, Room temperature operation of a single electron transistor made by the scanning tunneling microscope nanooxidation process for the TiO/Ti system, *Appl. Phys. Lett.* 68, 34 (1996): doi:101063/1, 116747.

[9] J. I. Shirakashi, K. Matsumoto, N. Miura, M. Kanagai, Single electron charging effects in Nb/Nb oxide-based single electron transistor at room temperature, *Applied Physics Lett.* 72, 15, 1893-1895(1998).

[10] Y. A. Pashkin, Y. Nakamura, J. S. Tsai, Room-temperature Al single electron transistor made by electron beam lithography, *Applied Physics Lett.* 76, 16,2256-2258(2000).

[11] J. R. Heath, M. A. Ratner, Molecular electronics, *Physics Today*, 56, 43-49(2003).

[12] A. K. Geim, K. S. Novoselov, The rise of grapheme, *Nature materials*, 6,183-191(2007).

[13] C. Wasshuber, Computational Electronics, New York: Springer-Verlag (2002).

[14] R. H. Chen, A. N. Karotkov, K. K. Likharev, A new logic family based on single electron transistors, *Proceedings of Device Res. Conf.*, 44-45, Charlottesville, 19-21 June 1995.

[15] K. Uchida, R. Matsuzawa, J. Koga, R. Ohba, S. Takagi, A. Toriumi, Analytical single electron transistor (SET) model for design and analysis of realistic SET circuits, *Jpn. J. Appl. Phys.*, 39,2321–2324(2000).

[16] Hiroshi Inokawa, Yamo Takashi, A compact analytical model for asymmetrical single-electron transistors, *IEEE Transactions on Electron Devices*, 50, 2,455-461(2003).

[17] S. Mahapatra, V. Vainish, C. Wasshuber, K. Banerjee, A. M. Ionescu, Analytical modeling of single electron transistor (SET) for hybrid CMOS-SET analog IC design, *IEEE Trans. Electron Devices*,51**,** 11**,**1772–1782(2004).

[18] S. Datta, Quantum Transport: Atom to Transistor, Cambridge University Press (2005).

[19] D. S. Hien, Development of quantum device simulator, NEMO-VN2, *Proceedings of fifth IEEE international symposium on electronic design, test and applications*, DELTA-2010, 13-15 January 2010, Ho Chi Minh City,170-173(2010).

Corresponding Author:
Le Hoang Minh
Ho Chi Minh City University of Technology and Education
Email: minhlh@hcmute.edu.vn