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A NOVEL OFFSET FUNCTIONS DESIGN FOR FIVE-LEVEL H-BRIDGE NPC INVERTERS TO REDUCE SWITCHING LOSS

ĐỀ XUẤT HÀM OFFSET GIẢM TỔN HAO DO SỰ CHUYỂN MẠCH CHO NGHỊCH LƯU CẦU H-NPC 5 BẬC

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ABSTRACT

This paper presents a new carrier pulse width modulator algorithm to reduce switching loss in five-level H-bridge neutral point clamped inverter. The proposed technique is based on the offset function being 3rd harmonic voltage. The offset voltage will be added to the control voltages so that the voltage of phase which has absolute of load current largest move into top (or bottom) of the carriers. So reducing the intersection of control voltage in that phase and the carriers and then reducing the number of switching losses. With the pulse width modulation method and flexible offset voltages in this study, switching loss in a cycle will be decrease. Simulation results will be provides in order to validate the proposed algorithm.

Keywords: *Carrier based pulse width modulation; offset function; reducing the number of switching losses; H-NPC inverter; five-level.*

TÓM TẮT

Bài báo này trình bày kỹ thuật điều chế sóng mang thông qua việc sử dụng hàm offset nhằm giảm tổn hao do sự chuyển mạch của các khóa công suất cho nghịch lưu cầu H-NPC 5 bậc. Kỹ thuật này sử dụng hàm offset là thành phần bậc 3 để chuyển các sóng điện áp điều khiển về ngưỡng cực đại hoặc cực tiểu của biên độ các sóng mang tại thời điểm dòng điện pha không đạt cực tiểu và biên độ dịch chuyển của điện áp điều khiển là cực tiểu. Khi điện áp điều khiển về ngưỡng cực đại hoặc cực tiểu của biên độ các sóng mang sẽ giảm giao cắt giữa sóng điều khiển và sóng mang để giảm số lần chuyển mạch ở vùng tổn hao do sự chuyển mạch lớn. Với kỹ thuật xây dựng hàm offset trình bày trong nghiên cứu, các khóa công suất đang chịu dòng tải lớn sẽ hạn chế chuyển trạng thái. Do đó tổng tổn hao do sự chuyển mạch sẽ giảm. Kết quả của giải thuật được kiểm chứng qua mô phỏng.

Từ khóa: *Điều chế sóng mang; hàm offset; giảm số lần chuyển mạch; nghịch lưu H-NPC; 5 bậc.*

1. INTRODUCTION

Multilevel inverters are power electronic converters that play important roles in applications of mechanical - electrical systems, transfortation, power quality management, renewable energy conversion such as solar energy, wind energy connected to electrical grids. Space-vector pulse width modulation and carrier based pulse width modulation are the typycal control techniques of inverters [1]. Because of industrial requirements, the inverters made with the capacity greater than [2]. Due to the increase in capacity of the inverters, the power loss becomes a problem that needed to solve.

It causes power losses in inverter including loss in power source (P_S), loss in wires (P_l), loss in control circuit (P_{Dr}), and loss in switches (P_{SW}) [3]. Of the power losses mentioned above, loss in switches is the largest, depending on modulation algorithm and topology [4]. The loss on switches of the inverter on a period of control voltage can be determined as (1):

$$P_{SW} = P_{SS} + P_{CS} \qquad (1)$$

Where P_{CS} and P_{SS} are conductive and switching loss of switches.

$$P_{SS} = \sum_{i=1}^{p} P_{S,i} \qquad (2)$$

$P_{S,i}$ is switching loss on the i^{th} switch; p are number of switches in topology.

According to [5], the switching loss on the i^{th} switch ($P_{S,i}$) depends on the number of switching in a control voltage cycle and is determined by the formula (3).

$$\mathbf{P_{S,i}} = \sum_{i=1}^{n} \mathbf{E_{ON}} \,.\, \mathbf{V_{CEi}}.\, \mathbf{I_{Ci}} + \sum_{j=1}^{m} \mathbf{E_{OFF}} \,.\, \mathbf{V_{CEj}}.\, \mathbf{I_{Cj}} \qquad (3)$$

Where n is the number times of status changed from OFF to ON; m is the same from ON to OFF. E_{ON} and E_{OFF} are the energies for switching ON and OFF, respectively. V_{CEi} and I_{Ci} are the voltage across power switch before conducting and the current after conducting at ON state i, respectively; V_{CEj} and I_{Cj} are the voltage across power switch after being OFF and the current before being OFF conducting at OFF state j, respectively.

Because V_{CEi}, V_{CEj} and supply voltage are equal, so that, reducing the switching or the switching takes place at a smaller of I_C, it will reduce switching losses. There are base of the algorithm to reduce witching loss. The study [5] shows reducing switching frequency often has the side effect is increased THD, so content paper proposes a new modulation technique reduces the number times of the switching on the phase that absolute of load current value is maximum. The proposed algorithm based on the use of the offset function put voltage control (which has maximum of absolution load current) on the top or bottom level of the carrier. Because the duration of each phase, reaching its absolute of load current on maximum, are the same and equal 1/3 cycle of control voltage, the number of switching will decreased about 33 percent. Proposed algorithm will be simulated on five-level H-bridge NPC topology in Mathlab and PSIM software.

2. TOPOLOGY OF FIVE-LEVEL BRIDGE H-NPC INVERTERS

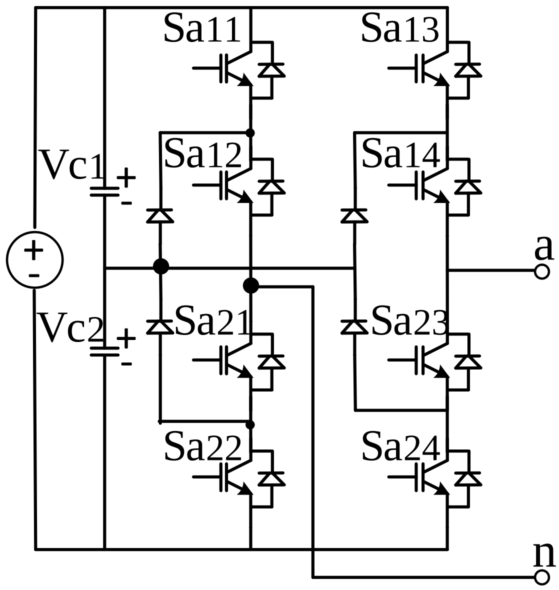


Fig. 1. *A phase of five-level H-bridge NPC inverter.*

Structure of a phase of five level H-bridge NPC inverter is in figure 1 [6]. Hence, the voltage from phase to pole (U_{xgj}) is determined by(4):

$$U_{xgj} = (T_{Sxj}).U_{xj} = (T_{SxTj} - T_{SxPj}).U_{xj} \qquad (4)$$

Where T_{Sxch} is defined in (5) with Ch=T, P (showed by left side branch and right side branch, respectively).

$$T_{Sxj} = T_{SxPj} - T_{SxTj} \qquad (5)$$

Where j is the index of switches (1 to 4) and T is the state of switch.

So, the phase to pole voltages is given by (6):

$$\begin{bmatrix} U_{ag} \\ U_{bg} \\ U_{cg} \end{bmatrix} = u_{dc} \begin{bmatrix} T_{SaT} & -T_{SaP} \\ T_{SbT} & -T_{SbP} \\ T_{ScT} & -T_{ScP} \end{bmatrix} \qquad (6)$$

The phase voltages and line to line voltages of five-level H-bridge NPC inverter is given by (7) and (8):

$$\begin{bmatrix} U_{an} \\ U_{bn} \\ U_{cn} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} U_{ag} \\ U_{bg} \\ U_{cg} \end{bmatrix} \quad (7)$$

$$\begin{bmatrix} U_{an} \\ U_{bn} \\ U_{cn} \end{bmatrix} = \frac{u_{dc}}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} T_{SaT} - T_{SaP} \\ T_{SbT} - T_{SbP} \\ T_{ScT} - T_{ScP} \end{bmatrix} \quad (8)$$

Thus, phase to pole voltages U_{xg} and line to line voltages U_{xy} have the third order harmonic while the phase voltage U_{xn} do not. Therefore, it can be seen that if offset function in the proposed algorithm of inverter control which is the third order harmonic will not affect the magnitude of the third order harmonic of the load. Besides, the phase to pole voltage U_{xg} will have 5 level including two positive levels, two negative levels and zero. There are ±2U, ±U, and 0.

3. CARRIER PWM ALGORITHM TO REDUCE THE NUMBER OF SWITCHING

This CPWM algorithm proposed in [7]. The main idea in this algorithm is add a third order harmonic, called offset voltage, to control signal, with the aim of reducing the switching of the leg phase has difference between the control voltages and nearest carriers is the smallest. Call v_x is voltage to control x phase, and v_{rx} is calculated control voltage from the PWM modified algorithm to reduce switching frequency. The principle of this algorithm was showed in Fig 2 [7].

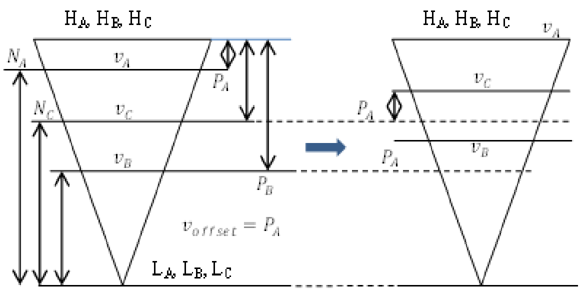


Fig. 2. *Principle of the CPWM algorithm to reduce number of switching [7]*

The simulation results show that this algorithm allows reducing the switching of the leg phase that different of control voltages of it with nearest carrier is smallest. Therefore switching can do on the phase that has load current (absolute) being smallest. So switching loss is not minimums. Then it is necessary for the proposed algorithm to reduce switching in the phase which load current (I_C) none smallest. This is the ideal solution to reduce energy losses due to switching without sacrificing THD as prescribed.

4. PROPOSED ALGORITHM

4.1. The principle of algorithm

On 3-phase five-level H-bridge NPC inverter, because the voltage across the switchV_{CEi} and V_{CEj} is always U_{DC} / 2, so the switching loss depends on current through power switches and the number of switching in the period of control voltage [8]. Thereby reducing the switching on the phase has maximum (priority first-if can) or medium (priority second) of absolution load current. Define: v_x is control voltage initial phase x, v_{rx} is calculated control voltage from algorithm. Select 0 is the bottom of the carrier with the smallest amplitude and peak amplitude of the triangle carrier waves are equal and equal to 1, then this time the threshold comparison of the carrier will be 0, 1, 2, 3 and 4. The control voltage of phase x is v_x is determined by (9).

$$v_x = v_{1,x}\cos(\omega t + j_x) + 2 + v_{offset} \quad (9)$$

Define L_x and ε_x as follows:

$$L_x = \begin{cases} int(v_x)\ if\ int(v_x) < 4 \\ int(v_x) - 1\ else \end{cases} \quad (10)$$

$$e_x = v_x - L_x \quad (11)$$

Call I_{xABS} is the absolute value of current across phase x.

And define the matrixes as (12 to 17)

$$[I_{max}] = [amax,\ \ bmax,\ \ cmax] \quad (12)$$

$$xmax = \begin{cases} 1\ if\ I_{xABS} = \max(I_{aABS}, I_{bABS}, I_{cABS}) \\ 0\ else \end{cases}$$

$$[I_{min}] = [amin,\ \ bmin,\ \ cmin] \quad (13)$$

$$xmin = \begin{cases} 1 \; if \; I_{xABS} = \min(I_{aABS}, I_{bABS}, I_{cABS}) \\ 0 \; else \end{cases}$$

$$[I_{med}] = [amed, \quad bmed, \quad cmed] \qquad (14)$$

$$xmed = 1 - xmax - xmin$$

$$[E_{max}] = [eamax, \quad ebmax, \quad ecmax] \qquad (15)$$

$$exmax = \begin{cases} 1 \; if \; e_x = \max(e_a, e_b, e_c) \\ 0 \; else \end{cases}$$

$$[E_{min}] = [eamin, \quad ebmin, \quad ecmin] \qquad (16)$$

$$exmin = \begin{cases} 1 \; if \; e_x = \min(e_a, e_b, e_c) \\ 0 \; else \end{cases}$$

$$[E_{med}] = [eamed, \quad ebmed, \quad ecmed] \qquad (17)$$

$$exmed = 1 - exmax - exmin$$

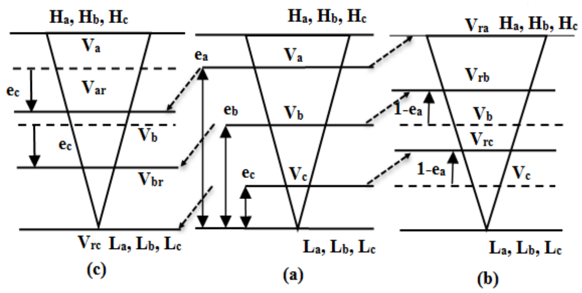


Fig. 3. *Principle of the proposed algorithm*

So that with v_a, v_b, and v_c showed in fig 3a, there are four cases and then we can decide offset voltage as in table 1

Table 1. *State of the proposed algorithm*

Case	Conditions	Fig	Offset
1	amax=1; eamax=1	3b	1-e_a
2	cmax=1; ecmin=1	3c	-e_c
3	bmax=1; ebmed=1; amed=1	3b	1-e_a
4	bmax=1; ebmed=1; cmed=1	3c	-e_c

So general offset function is determined as (18).

$$\begin{aligned} v_{offset} &= -e_{min}.([I_{max}].[e_{min}]^T \\ &+ [I_{max}].[e_{med}]^T.[I_{med}].[e_{min}]^T) \\ &+ (1 - e_{max}).([I_{max}].[e_{max}]^T \\ &+ [I_{max}].[e_{med}]^T.[I_{med}].[e_{max}]^T) \end{aligned} \qquad (18)$$

Control voltage (v_{rx}) after added offset will move to the new location inside phase has minimum of offset and the absolute value of the load current being maximum or medium. (Figure 4)

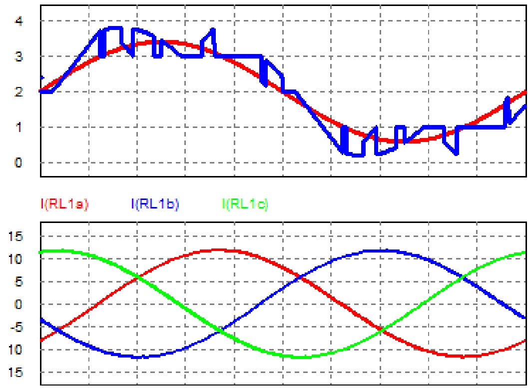


Fig. 4. *controlled Voltage initially and after applied the proposed algorithm m=0.7.*

Formula (18) may seem complicated, but the elements of the matrixes are only valid "0" and "1" so the calculation will be very fast and easy.

4.2. Flow chart

From 4.1. the flow chart of proposed algorithm built as figure 5. The flow chart shows that the proposed algorithm uses simple commands as plus, minus, comparison of the program.

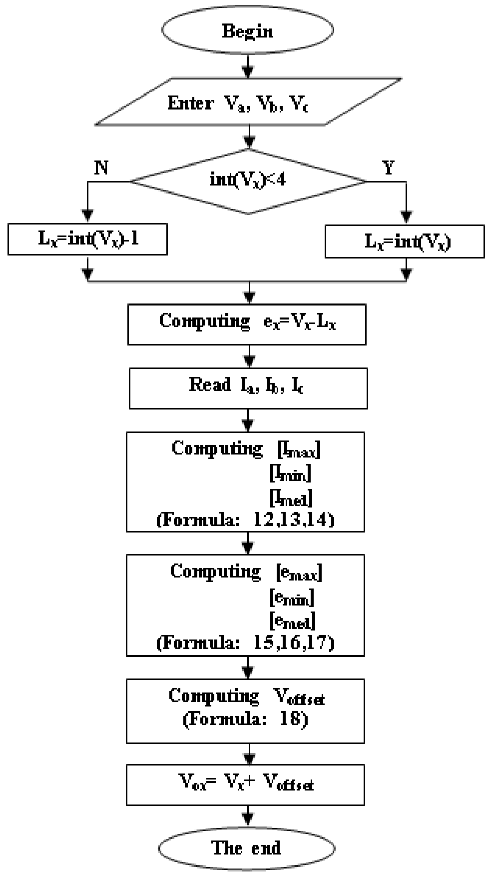


Fig. 5. *The proposed flow chart*

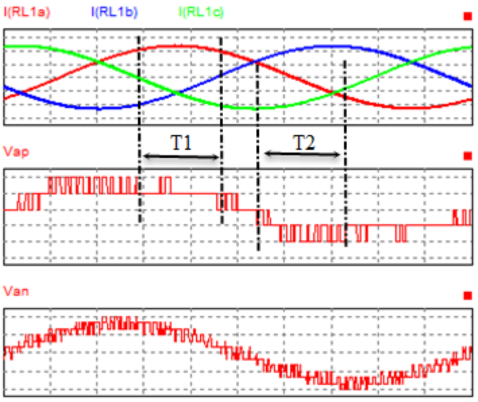
The comparison of the phase currents can be done by comparing circuits (hardware and does not require use of expensive sensors). Thus, calculation time is low, suitable for closed-loop control or other control methods.

5. SIMULATIONAND EXPERIMENTAL RESULTS

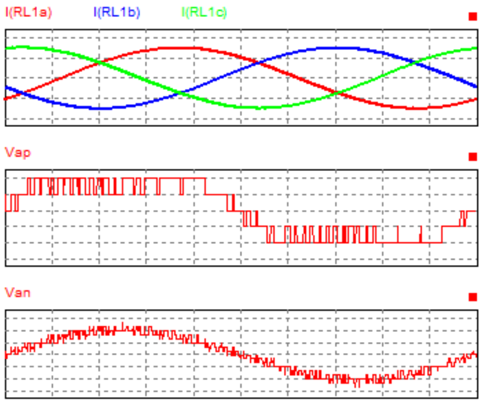
The proposed algorithm will be proven on model five level H-bridge NPC inverter having a 100V DC voltage source, the carrier frequency of 3000Hz, a three-phase load balance of R = 10Ω, L = 30mH.

Figure 6 are simulation results at modulator index m=0.7 and m=0.9.

The simulation results show that when the absolute of phase current "A" reach maximum (some time medium) – T_1, then switching on the phase is lower than it when phase current near zero (T_2).



(a)m = 0.7



(b)m = 0.9

Fig. 6. *The results of the simulation proposed algorithm.*

The same things are happening when m=0.9. Therefore considering modified algorithm reduces the number of switching then this algorithm also reduces the switching similar and it is about 30%. So certainly, losses due to the switching will be smaller too. At modulation index m = 0.9, the total harmonic distortion (THD%) of phase voltage go respectively 6.03% and lower than the required under the present in standards of Vietnam (TCVN-7909 2.2-2008) and also meet the standards EMS according to international standards EN6100-2-2 (Figure 6).

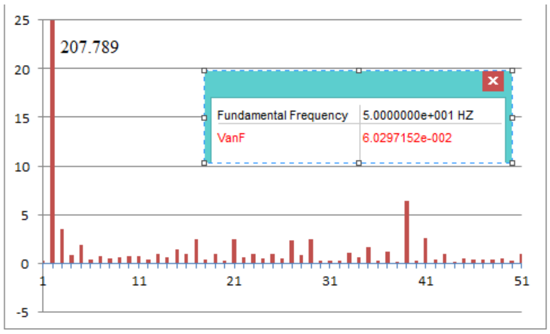


Fig. 7. *Analyze the THD of phase voltage applied proposed algorithm index m = 0.9*

Figure 8 is the comparison between the proposed algorithm and minimum common mode algorithm of Total Harmonic Distortion (THD) of phase voltage. Results in Figure 8 shows that Total Harmonic Distortion (THD) of phase voltage applied propose algorithm is greater than in applied minimum common mode algorithm at the same modulation index. However, with the modulation index m≥0.5 proposed algorithm get value total harmonic distortion is smaller than the standards of Viet Nam.

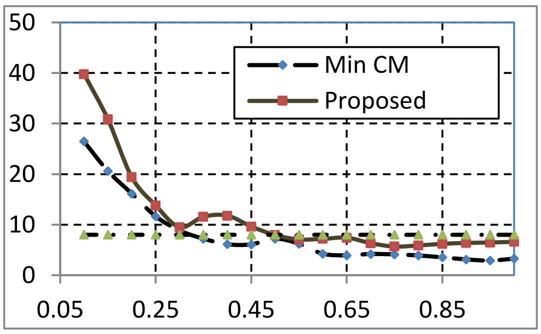


Fig. 8. *Relations modulation index and THD% phase voltage applied propose and minimum common mode algorithms*

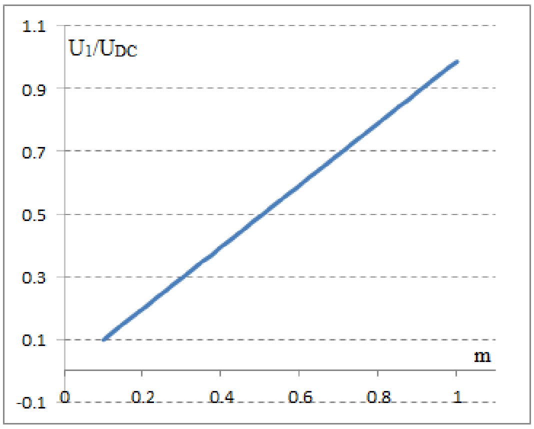


Fig. 9. *Control characteristics*

The control characteristic of the proposed algorithm is nearly linear and similar to that of medium common mode algorithm (Figure 9). Control characteristic of proposed algorithm and it of [10] are the same. Figure 10 shows a comparison of the number of times switching per cycle control voltage applied propose algorithm and minimum common mode algorithm with carrier frequency is 3 kHz.

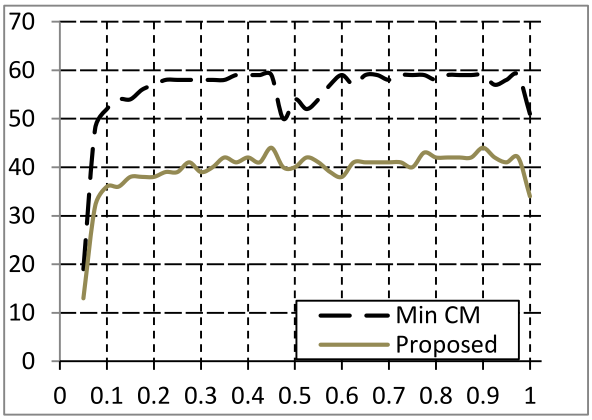


Fig. 10. *The number of times switching in period of control voltage applied proposed and minimum common mode algorithms.*

The number of switching on the proposed algorithm is lower than that of medium common mode algorithm by 33.33% corresponding decrease 1/3 switching frequency and it same when applied the algorithm [3].

6. CONCLUSIONS

The paper presents the carrier based pulse width modulation algorithm by using offset function to reduce the number of commutations of power switches in bridge H-NPC five-level inverters special reduced switching positions of the phase having maximum of absolute of phase current therefore proposed algorithm can reduce switching losses. This algorithm can not only reduce the number of switching, but also select phase having larger current for reduce of switching.

With proposed algorithm, we only need to determine the phase that having the largest, smallest and average of the current phase. So that, we can use the logic circuits and no need to use ADC. These lead to reduced hardware costs and increase computing speed.

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