MODELING AND SIMULATIONS OF METALLIC AND SEMICONDUCTING SINGLE ELECTRON TRANSISTORS

MÔ HÌNH VÀ MÔ PHỎNG TRANSISTOR ĐƠN ĐIỆN TỬ KIM LOẠI VÀ BÁN DẪN

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ABSTRACT

Single electron transistor (SET) is a key element in current research area of nanoelectronics which can offer nano-feature size, low power consumption and high operating speed. SET could be promising alternative for MOSFET in the future. The goal of this paper is to discuss about recent advances in fabrication of the SETs and focuses on simulation of their basic quantum device characteristics like tunneling effect, Coulomb blockage, Quantum dot, Coulomb staircase, and Coulomb oscillation. Some results of simulation of two types of metallic and semiconducting SETs have been obtained.

Keywords: *single electron transistor; current-voltage characteristics; Coulomb blockage; Coulomb staircase; Coulomb oscillation; metallic and semiconducting SETs.*

TÓM TẮT

Transistor đơn điện tử (SET) là một yếu tố cơ bản trong lĩnh vực nghiên cứu về điện tử nano hiện nay. SET cho kích thước đặc tính nano, tiêu tốn công suất thấp và tốc độ làm việc cao. SET có thể là sự thay thế hứa hẹn cho MOSFET trong tương lai. Mục tiêu của bài báo này là bàn về những tiến bộ trong chế tạo SET và tập trung lên mô phỏng đặc trưng lượng tử cơ bản của linh kiện như hiệu ứng xuyên hầm, khóa Coulomb, chấm lượng tử, bậc thang Coulomb và dao động Coulomb. Một số kết quả mô phỏng hai loại SET "kim loại" và "bán dẫn" đã nhận được.

Từ khóa*:Transistor đơn điện tử; đặc trưng dòng-thế; khóa Coulomb; bậc thang Coulomb; dao động Coulomb; SET "kim loại" và SET "bán dẫn".*

1. INTRODUCTION

Single electron transistor (SET) holds great promising for future nanoelectronics and nanotechnology due to their nano size, ultra-low power dissipation and high frequency. In the future it is probable that the nano-MOSFETs could be replaced by new fundamental device like single electron transistor. SETs have attracted much attention for IC applications because of new functionalities, and CMOS compatible fabrication process [1].

After their discovery in the 1986 [2, 3], there has been extensive research on fabrication, design and modeling of SETs [4]. SETs with a variety of structures were proposed and fabricated by using different

methods [5-7]. SETs have been fabricated to operate at room temperature [8-10]. Molecular quantum dot [11] can display SET's behavior. 1D structures, such as carbon nanotubes and nanowires, can act as SETs [7]. Recent advances in grapheme [12] show promise for SETs.

Research on SET modeling and simulation has been an active area. Monte Carlo simulation has been widely used to model SETs. SIMON [13] and MOSES [14] are the two most popular SET simulators. Uchida et al. proposed an analytical SET model and incorporated it into SPICE [15]. Inokawa et al. extended this model to a more general form to include asymmetric SETs [16]. Mahapatra et al. proposed a simulation framework for hybrid SET/CMOS circuit design and analysis [17]. In contrast, model used non-equilibrium Green's function method (NEGF) [18] commonly used in the nanoscale devices and are superior in terms of simplicity.

In this work, we introduce modeling of SET and simulate current-voltage characteristics in single electron transistor by non-equilibrium Green's function method using graphic user interface (GUI) of Matlab. Here, we use a model inone level mode for the metallic SET and multiple level mode for the semiconducting SET (i.e. it takes quantization into account in quantum dot). We also summarize the theoretical approach based on NEGF, review the capabilities of the simulator, NEMO-VN2 [19], give examples of typical simulations of SET's current-voltage characteristics.

2. MODELING AND SIMULATION OF ONE LEVEL AND MULTIPLE LEVEL SETs

As shown in Figure 1 a SET typically has three terminals. The source and drain terminals serve as electron reservoirs. When the SET is turned on, electrons tunnel from one terminal, through the junction, to the conductive or semiconducting island. They then tunnel through the other junction to the other terminal. Each tunneling junction is modeled as resistor (R_S or R_D) and capacitor (C_S or C_D) in parallel.A gate terminal (G), with coupling capacitance C_G, controls the transport of electrons. Electrons can therefore tunnel, in single-file, through the island as determined by V_{DS}.

In order to observe the Coulomb blockade effect, the following constraints must be satisfied.

1) Since thermal fluctuations can suppress the Coulomb blockade effect, the electrostatic charging energy, e^2/C_Σ, must be much greater than k_BT, where k_B is Boltzmann's constant and T is the temperature. In order to ensure reliability, $e^2/C_\Sigma \geq k_B T$ other more conservative, $e^2/C_\Sigma \geq 40k_B T$ constraint is enforced. These equations imply that the maximum allowed island capacitance is inversely proportioned to temperature. At room temperature, an island capacitance below 1 aF is required. Island capacitance is function of island size. Room temperature operation requires an island size in the nanometer range, making fabrication challenging. At present, the smallest island capacitance of a fabricated device is around 0.15 aF [9].

2) To observe single-electron charging effects, electrons must be confined to the island, which requires that the junction resistance be higher the quantum resistance, i.e., R_S, $R_D > h/e^2$, h/e^2 = 25.8 kΩ, where h is Plank's constant. Therefore, SETs have high resistances and low driving current.

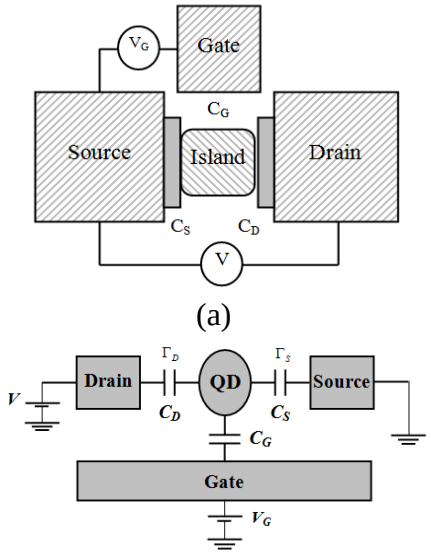

Figure 1. *(a) Structure of SET, (b) equivalent schematic diagram of SET: C_G - gate capacitance, C_S - source tunnel junction capacitance, C_D – drain tunnel junction capacitance, R_S – source tunnel junction resistance, R_D – drain tunnel junction resistance.*

In order to operate voltage-state logic, SETs must exhibit voltage gain. The low-temperature voltage gain is equal to the gate capacitance divided by the sum of the junction capacitances: $G = C_G/(C_S+C_D)$. Achieving this gain requires low tunneling junction capacitances. It also requires close coupling of gate and island without a large increase in the total island capacitance. High gain has only been demonstrated for a few devices and has required operation at low temperature. However, further advances in nanofabrication may overcome this limitation.

There are a variety of materias chosen for fabrication of single electron transitors. Basing on fabrication of SETs [5-12], there are two categories of single electron transistors fabricated today, "metallic" and "semiconducting", therefore we use two modes of modeling: one level and a multiple level respectively.

Here, we describe SET's model for one level and a multiple level device whose energy levels are described by a Hamiltonian matrix [H] and whose coupling to the source and the drain contacts is described by self-energy matrices $[\Sigma_1(E)]$ and $[\Sigma_2(E)]$ respectively (Figure 2).

The flow of current is due to the difference in potentials between the source and the drain, each of which is in a state of local equilibrium, but maintained at different electro-chemical potentials $\mu_{1,2}$ and hence with two distinct Fermi functions:

$$f_1(E) = \frac{1}{exp\left[{}^{(E-\mu_1)}/_{k_BT}\right]+1} \quad (1)$$

$$f_2(E) = \frac{1}{exp\left[{}^{(E-\mu_2)}/_{k_BT}\right]+1} \quad (2)$$

by the applied bias V: $\mu_2 - \mu_1 = -qV$. Here, E- energy, k_B - Boltzmann constant, T-temperature.

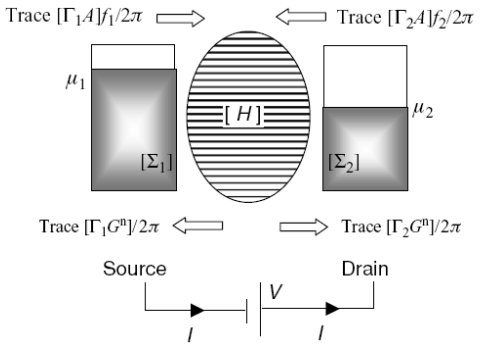

Figure 2. *Multi-level device whose energy levels are described by a Hamiltonian matrix [H] and whose coupling to the source and drain contacts is described by self-energy matrices $[\Sigma_1(E)]$ and $[\Sigma_2(E)]$ respectively.*

The density matrix is given by

$$\rho = \int_{-\infty}^{+\infty} \frac{dE}{2\pi} G^n(E) = \int_{-\infty}^{+\infty} \frac{dE}{2\pi} [A_1(E)f_1(E) + A_2(E)f_2(E)] \quad (3)$$

The current I_D flows in the external circuit is given by Landauer formula [8]:

$$I_D = (q/h) \int_{-\infty}^{+\infty} dET(E)\big(f_1(E) - f_2(E)\big) \quad (4)$$

The quantity T(E) appearing in the current equation (4) is called the transmission function, which tells us the rate at which electrons transmit from the source to the drain contacts by propagating through the device. Knowing the device Hamiltonian [H] and its coupling to the contacts described by the self-energy matrices $\Sigma_{1,2}$, we can calculate the current from (4). For coherent transport, one can calculate the transmission from the Green's function method, using the relation:

$$T(E) = Trace[\Gamma_1 G \Gamma_2 G^+] + Trace[\Gamma_2 G \Gamma_1 G^+] \quad (5)$$

The appropriate NEGF equations are obtained:

$$G = [EI - H - \Sigma_1 - \Sigma_2]^{-1},$$

$$\Gamma_{1,2} = i\left[\Sigma_{1,2} - \Sigma_{1,2}^{+}\right], A_1(E) = GI,$$

$$G^n = [A_1]f(E) + [A_2]f(E),$$

$$A = i[G - G^+] = [A_1] + [A_2] \quad (6)$$

Where H is effective mass Hamiltonian, I is an identity matrix of the same size, $\Gamma_{1,2}$ are the broadening functions, $A_{1,2}$ are partial spectral functions, A(E) are spectral function, G^n is correlation function. We use a discrete lattice with N points spaced by lattice spacing a to calculate the eigenenergies for electrons in the quantum dot.

By utilizing the simulator namely NEMO-VN2 [19], the I_D–V_G characteristics of metallic SET inone level mode having the given parameters are shown in Figure 3.

Figure 3 demonstrates the typical Coulomb oscillation behavior in SET I_D-V_G characteristics. It shows that the SET Coulomb oscillation period (e/C_G, e is the electronic charge) is dictated by SET's gate capacitance. Values of gate voltage at the first and the second peaks are e/2C_G (80 mV) and 3e/2C_G (240 mV) respectively. Here, it should be emphasized that the peak and the valley currents of Coulomb oscillations are perfectly represented by the model. The results calculated according to model (e/2C_G for C_G = 1 aF) coincide well with the simulated ones.

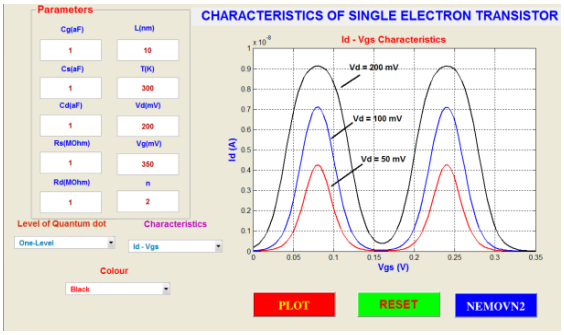

Figure 3. *I_D-V_G characteristics (Coulomb oscillations) of SET in one level for various values of V_D = 50 mV, 100 mV and 200 mV at room temperature, T = 300K. The SET parameters are: L = 10 nm, C_G = C_S = C_D = 1aF and R_S = R_D = 1 MΩ.*

Current-voltage (I_D-V_G) characteristics showing the suppression of the Coulomb oscillation by broadening current peaks increased at high V_D (200 mV). It also reveals the fact that it is difficult to obtain the Coulomb oscillations in the device characteristics at high V_D greater than 3e/C_T (C_T is total capacitance of SET), (160 mV). It should note that high drain voltage, V_D undermines SET's current-voltage characteristics. It notes that the drain saturation current, Id in multiple level (semconducting SET) is less than in one level (metallic SET) of 10 times.

Figure 4 shown the Coulomb oscillation behavior in SET I_D-V_G characteristics in multiple level (semiconducing SET). It shows that the SET Coulomb oscillation period (e/C_G, e is the electronic charge) is dictated by SET's gate capacitance. Values of gate voltage at the first and the second peaks are e/2C_G (80 mV) and 3e/2C_G (240 mV) respectively. Here, it should be emphasized

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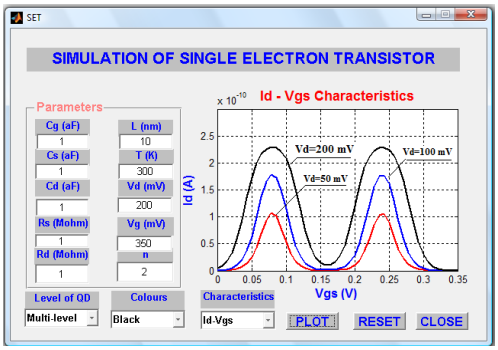


Figure 4. *I_D-V_G characteristics (Coulomb oscillations) of SET simulated by the simulatorNEMO-VN2 in multiple level for various values of V_D = 50 mV, 100 mV and 200 mV at room temperature, T = 300K. The SET parameters are: L = 10 nm, $C_G = C_S = C_D$ = 1aF and $R_S = R_D$ = 1 MΩ.*

Fig.5 reproduces SET's I_D-V_D characteristics at room temperature (T = 300 K) for different gate biases, V_G = 0 mV and V_G=$e/2C_G$ (Coulomb oscillation) of semiconducting SET. For V_G = 0 mV, V_D starts from the Coulomb blockade region and increases (or decreases) through the single-electron tunneling region. For $V_G = e/2C_G$ (at the first Coulomb oscillation peak), I_D starts from zero and increases (or decreases) linearly. The threshold voltage of SET is $V_G = e/2C_G$.

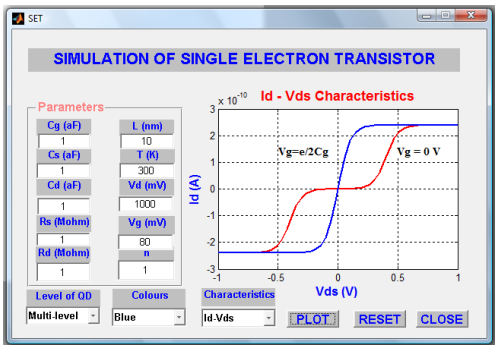
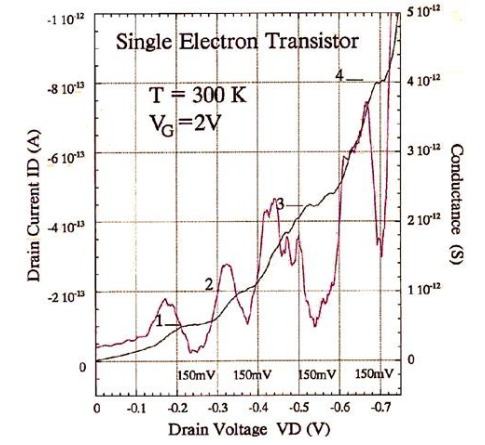


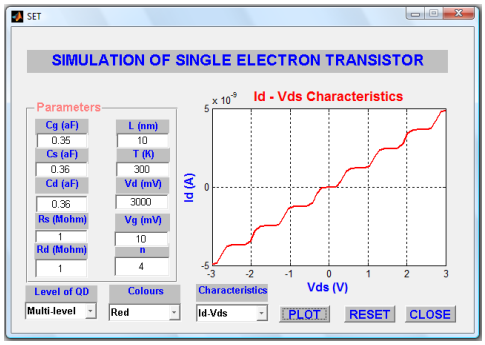
Figure 5. *I_D-V_D characteristics simulated by the simulator at room temperature T = 300 K for various values of V_G = 0 mV and $V_G = e/2C_G$ in multiple level. The SET parameters are: L = 10 nm, $C_G = C_S = C_D$ = 1 aF and $R_S = R_D$ = 1 MΩ.*

Accuracy of the model is evaluated by comparing simulated results with experimental ones from [8].

According to the work [8], its authors have succeeded in fabricating an SET. The SET operates at room temperature, showing a clear Coulomb staircase with a ~150 mV period at 300 K. The drain current-voltage characteristics of the SET were measured at room temperature and are shown in figure 6a. The gate bias was set to 2 V. In the Figure, the solid lines show the current of the SET, and the dashed line shows the conductance of the SET. Between the drain bias of 0 V and -0.75 V, four clear Coulomb staircases with a ~150 mV period are observed. The conductance oscillates with the increase of the drain bias with almost the same 150 mV period. The lower peaks of the conductance oscillation correspond to the flat regions of the current of the Coulomb staircase. The drain current versus gate bias characteristics with 150 mV drain bias at room temperature exhibit clear current oscillations with a period of ~460 mV, implying a periodic Coulomb oscillation of the current. The tunneling capacitance (C_t) and gate capacitance (C_g) could be roughly estimated from the period of the Coulomb staircase and oscillation. Their values were found to be C_t = ~3.6 x 10^{-19} F and C_G = ~3.5 x 10^{-19} F.Figure 5b,c reproduce I_D-V_D characteristics and conductance of the same SET having length, L = 10 nm at temperature of 300 K. Figures 6b,c show simulated results of I_D-V_D characteristics and conductance of the same SET.



a)



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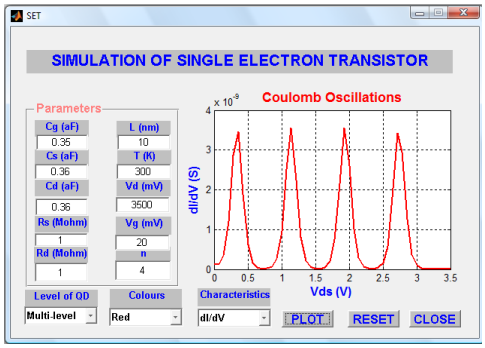

c)

Figure 6. *a) Drain current versus drain voltage characteristics of the SET at 300 K [8]: V_D = 150 mV, C_t = 0.36 aF, C_G = 0.35 aF; b) I_D-V_D characteristics simulated; c) Conductance characteristics simulated by the simulator, NEMO-VN2 for value of V_G = 20 mV. The SET device parameters are: L = 10 nm, C_G = 0.35 aF, C_S = C_D = 0.36 aF and R_S = R_D = 1 MΩ.*

Four clear Coulomb staircases are shown in simulated results on I_D-V_D characteristics (Figure 6b). Four clear conductance peaks are also shown in Figure 6c. The results simulated according to the model coincide well with the experimental ones.

3. CONCLUSIONS

Basic physical properties, fabrication, and the most popular simulators of SET have been introduced. A model for SET device using NEGF written in GUI of Matlab has been reported. The proposed model has been verified at multiple level for SET's device. A set of simulations is then successfully performed for various parameters of the SET's device in one level mode (metallic SET) and in multi-level mode (i.e. it takes quantization into account in the quantum dot, semiconducting SET). The model is not only able to accurately describe I_D-V_G, I_D-V_D SET's characteristics, but also affects of gate materials, size of SET, temperature on SET's characteristics. Different SET's device characteristics (I_D-V_G, I_D-V_D, effect of temperature) have been simulated. The simulated results are also compared with experimental ones [8] and good agreements are validated.

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