SI NANOWIRES GROWN BY Al-CATALYZED PLASMA-ENHANCED CHEMICAL VAPOR DEPOSITION (PECVD) ON QUARTZ SUBSTRATES FOR SOLAR CELL APPLICATIONS

DÂY NANO SILICON MỌC TỪ NHÔM XÚC TÁC TRÊN CƠ SỞ THIẾT BỊ LẮNG ĐỌNG PHA HƠI HÓA HỌC SỬ DỤNG PLASMA (PECVD) TRÊN ĐẾ THẠCH ANH CHO ỨNG DỤNG TẾ BÀO PIN NĂNG LƯỢNG MẶT TRỜI

Le Duc Toan
Phu Yen University, Vietnam

Received 05/03/2017, Peer reviewed 10/06/2017, Accepted for publication 30/6/2017

ABSTRACT

Silicon nanowires have been synthesized on quartz substrates using Al as a catalyst. Silane (SiH_4) diluted in H_2 carrier gas was employed as Si precursor in a plasma enhanced chemical vapor deposition (PECVD) system operated at 550°C. This growth temperature is lower than the eutectic temperature in the Al – Si system (577°C) which suggests a vapor – solid – solid (VSS) growth mechanism. Electrical measurements and back-gated current-voltage measurements indicated that silicon nanowires were heavily doped (p type), with a doping concentration of a few $10^{19}cm^{-3}$. We have measured hole mobility values of ~ $30cm^2/V.s$. We have also evaluated the use of those highly doped Si nanowires for solar cell applications based on core-shell structure, an efficiency of ~ 2,37% for the best one with fill factor of ~ 48,2%, open circuit voltage of ~ 0.70V and current density of ~ $15,2mA/cm^2$.

Keywords: *Silicon; nanowires; Silicon nanowires; solar cells; photovoltaics (PVs).*

TÓM TẮT

Dây nano silicon đã được tổng hợp trên đế thạch anh dùng nhôm như vật liệu xúc tác. Trong quá trình mọc khí silane (SiH_4) được trộn trong khí mang hyđrôgen (H_2) làm việc như một nguồn cung cấp silicon trong thiết bị lắng đọng pha hơi hóa học sử dụng plasma (PECVD) ở 550^oC. Nhiệt độ mọc này thấp hơn nhiệt độ cùng tinh (eutectic) của hợp kim Al-Si (577^oC) điều này đã gợi ý cơ chế mọc được thực hiện trong trường hợp này là cơ chế hơi – rắn – rắn (Vapor-Solid-Solid). Việc đo đặc tính điện, đặc trưng dòng thế thông qua cực cổng của transistor đã xác thực rằng dây nano silicon sau khi mọc là loại p-type và có nồng độ pha tạp khá cao khoảng $10^{19}cm^{-3}$. Độ linh động lỗ trống khoảng $30cm^2/V.s$. Chúng tôi đã phát triển sử dụng những dây nano silicon có nồng độ pha tạp cao loại p-type này cho các ứng dụng tế bào pin năng lượng mặt trời trên cơ sở cấu trúc lõi-vỏ, kết quả một hiệu suất khoảng 2,37% đã được tạo ra với các thông số fill factor khoảng 48,2%, điện thế lúc mạch mở V_{oc} ~ 0,7V và mật độ dòng khoảng $15,2mA/cm^2$.

Từ khóa: *Dây nano; silicon; Dây nano silicon; tế bào pin năng lượng mặt trời; quang điện.*

1. INTRODUCTION

Silicon nanowires (SiNWs) with excellent properties for photovoltage (PV) applications such as reflection reduction, extreme light trapping, absorption increasing, defect tolerance, less material use… in recent years, solar cells based on c-Si micro/nanowire arrays have emerged [1–5] as an alternative orientation for high cost traditional mono c-Si wafer solar cells (first generation of solar cells). This is reason why SiNWs have attracted a great deal of attention as one of the most promising building blocks for submicron electronic device applications in general, especially for solar cells.

Although SiNWs can be fabricated by top-down microelectronic technologies (extensively based on photolithography and etching) [6–9], in many cases, they are grown from colloidal nanoparticles, using the so-called vapor-liquid-solid (VLS) process, which can be implemented in a chemical vapor deposition (CVD) reactor [10,11]. For Si NWs synthesis, the VLS process starts with the formation of a liquid alloy (usually a low-melting point eutectic composition) between a catalyst material (preferably a metal such as gold) and the semiconductor atoms originating from the decomposition of a gaseous precursor such as SiH_4. This is followed by Si precipitation from the supersaturated eutectic alloy and the one-dimensional growth of nanowires [12].

In addition to the VLS growth, nanowires can grow through a vapour-solid-solid (VSS) mechanism involving a solid catalyst particle. As far as Si is concerned, VSS growth has been reported in several studies such as the synthesis of $TiSi_2$-catalyzed SiNWs [13], Pd-catalyzed SiNWs [14] and Al-catalyzed SiNWs [15]. Schematically, NWs grow according to the VLS mechanism when the growth temperature is higher than the catalyst-semiconductor eutectic temperature, whereas they follow the VSS route when the growth temperature is lower than the eutectic temperature. Au has been extensively used as a catalyst for the VLS synthesis of Si nanowires since it does not oxidize and provides a low temperature (~365°C) Au-Si eutectic point. However, in silicon technology, Au is well known as a lifetime killer for carriers in solar cells applications, since it forms deep trap levels inside the Si forbidden band gap [16]. Of course such a situation should be avoided, particularly when minority carrier devices are of concern (*e.g.*, solar cells). Also, Si NWs grown from an Au catalyst are intrinsic or non-intentionally doped, unless dopant gas sources such as phosphine (PH_3) or diborane (B_2H_6), for n type or p type doping respectively, are added in the gas phase during growth. However, the addition of those dopant gases can produce non uniform radial dopant profiles [17–19], as well as reduce the nucleation yield and the growth rate of the SiNWs. For all the above reasons, aluminum (Al) [15,20–22], together with other "CMOS-friendly" catalysts [13,23] have been studied over the past few years. The Al-Si and Au-Si phase diagrams are very similar, but the major difference is the high Al reactivity towards ambient O_2 and H_2O, leading to the almost unavoidable formation of surface Al_2O_3, which tends to block Si diffusion [24], thus preventing Si from mixing with Al. For this reason, the growth of Al-catalyzed SiNWs is preferably performed in ultra-high vacuum environments, using *in situ* Al deposition [20–22,25]. One of the peculiarities of the Al catalyst (a column III element) is that there is no need of dopant gas in the growth atmosphere (such as B_2H_6 or trimethyl boron), since it directly produces

p-doped SiNWs. Another advantage is that the dopant profile (*i.e.*, Al itself in this case) is uniform along the radial and axial directions of the Si wire [16].

In this work, we have use a plasma-enhanced chemical vapor deposition process (PECVD) to grow the SiNWs from Al thin films directly deposited on quartz substrates, the Al-catalyzed SiNWs thus obtained have been characterized by scanning electron microscopy (SEM), transmission electron microscopy (TEM) and electrical measurements, including field- effect transistor evaluations. Having precisely evaluated the electrical characteristics of those Al-catalyzed SiNWs, we have studied their application to solar cells with core-shell structure.

2. METHODS

2.1. Growth of the Al-catalyzed SiNWs on quartz substrate

Depend on the purpose for using, we can grow SiNWs on different substrates, for example: silicon, stainless steel or quartz substrates…, and in this case we chose quartz substrates because of low cost and its tough quality during process for solar cell fabrication. First of all, we prepared quartz substrates in size of $1cm^2$. The substrates were then cleaned in solvent solution (acetone, isopropanol and ethanol) to remove all dirty and organic particles prior to the deposition of a 300 nm-thick Al film coating by high vacuum electron-beam evaporation (in this case, we used a thick aluminum film of 300nm for electricity conducting purpose (back contact for the solar cell)), on other hand this aluminum film also kept the role as a catalyst metal film for SiNWs growth. The Al-coated quartz substrates were then loaded on the bottom electrode (sample-holder/heater) of the PECVD reactor which was pumped down to ~ 10^{-6} torr. Once the base pressure reached, the temperature of the sample-holder was set to 550°C and H_2 gas was introduced into the chamber, at a flow rate of 250sccm while the pressure was stabilized and maintained at 0.5torr. Then, the plasma was ignited and sustained for the next 20min, with a 20W applied power. During this step, the H_2 – based plasma generates atomic hydrogen, which helps cleaning the Al surface and reducing the native Al_2O_3. After 20min, as the temperature had stabilized at 550^oC, SiH_4 was introduced into the chamber at flow rate of 25sccm, while the H_2 flow was kept unchanged then the growth of the SiNWs started to proceed. After growth termination, the temperature was decreased down to room temperature and the samples were unloaded from the reactor. The nanowire morphology was first observed by scanning electron microscopy (SEM); some specimens were transferred onto Cu grids and then observed by transmission electron microscopy (TEM).

2.2. Electrical characterizations of the Al-catalyzed SiNWs

After growth, the nanowires were solubilized into an isopropyl alcohol solution through sonication. They were subsequently drop-casted onto a SiO_2/ Si substrate (p-type, 0.005Ω.cm with a 300nm thermal SiO_2 layer). A number of device structures such as field-effect transistors (FETs) were fabricated and tested. When tested in FET configuration, the highly-doped Si substrate under the oxide was used as a back gate. Photolithography was used to define the locations of 2 electrodes, in order to contact each nanowire (figure 6). After a 10s dip in buffered oxide etchant, which removed the native oxide from the surface of the nanowires, the samples were immediately loaded into an evaporator chamber to deposit 150nm Ni + 50nm Au films. Following metal deposition, the samples were dipped in acetone in order to

remove the photoresist and the unwanted metal (lift-off process). Finally, the devices were annealed at 350°C during 10min to complete the device fabrication before investigating electrical properties. All electrical measurements were performed with a Keithley 4200-SCS Semiconductor Characterization System.

2.3. Solar cells fabrication and characterizations.

Based on SiNWs growth process, concerning solar cells applications, figure 1 explained clearly the process for fabricating the solar cell devices: quartz substrates after cleaning (figure 1a) were deposited 300nm Al (figure 1b), an area of Al was etched out of the sample device's surface via photolithography and remained an area of Al with the shape of 0,25x0,75cm^2 (figure 1c-d), next we used another small quartz wafer to cover on a part of Al film with an area of 0,25x0,5cm^2 where we were going to use as the back contact for the cell, this helped to protect the aluminum film below that quartz wafer in growth duration (figure 1e) (silicon atoms could not drop on the aluminum surface below that quartz wafer to make Al-Si alloy so this part of aluminum kept quality as deposited), by this

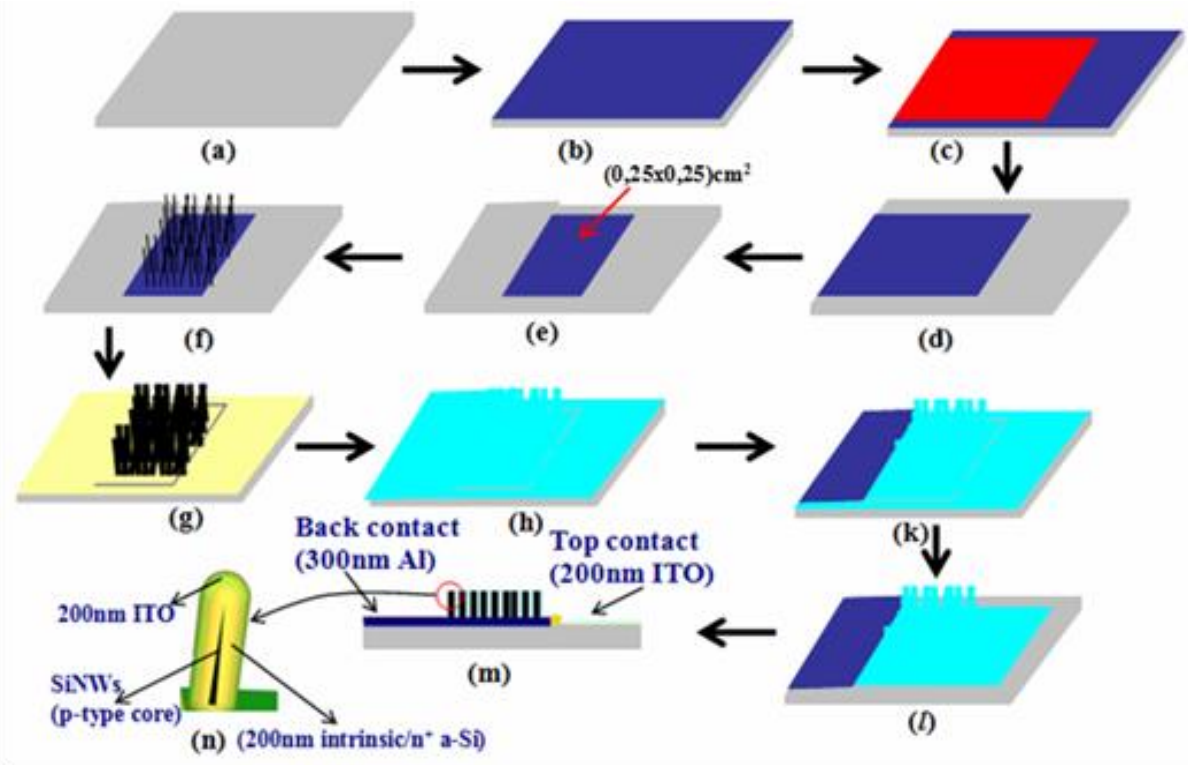

Figure 1. *The process to fabricate the solar cell device: (a) Quartz substrate after cleaning; b) Al film (300nm) was coated on quartz substrate; c) a photolithography process was made for etching unwanted aluminum on quartz substrate; d) Al remained after etching (0,25x0,75 cm^2); e) a small quartz substrate covered on a part of Al film, the Al film remained as the operation area of the cell (0,25x0,25cm^2); f) p-type core SiNWs grown on the operation area of the cell (0,25x0,25cm^2); g) 150nm intrinsic a-Si/50nm n$^+$-type a-Si was coated around p-type core SiNWs to make p-i-n structure; h) ITO film (200nm) was coated for top electrode of the cell; k) covering quartz substrate was removed from the sample device; l) unwanted ITO film was removed from the sample device's surface; m) cross section image of the completed solar cell device; n) structure of a p-i-n wire after ITO coating.*

way we defined the operation area of the cell is 0,25x0,25cm^2 (figure 1e). After the growth of the core p-type Si NWs (figure 1f), the SiH_4 as well as the plasma power was stopped and the reactor temperature was decreased to 200°C under H_2 flow. Once the temperature stabilized, SiH_4 was re-introduced in the reactor (20sccm) and the plasma ignited again and set to 20W; the total pressure was fixed at 300mTorr. In those conditions, a first shell of intrinsic, or rather non-intentionally doped (NID) hydrogenated amorphous Si (a-Si:H) was deposited all around the p-type Si wire cores. Once the desired thickness reached, (typically 150nm) all parameters were kept unchanged and PH_3 (0.05% diluted in H_2) was flowed into the reactor (40sccm), in order to realize a second n^+-doped shell layer, typically 50nm-thick (figure 1g). Using the ImageJ software, we evaluated the area covered by p-i-n nanowires to ~ 97% of the footprint of the Al electrodes. After growth of p-i-n wires, the samples were loaded out from PECVD systems, and slowly moved inside Sputtering system to deposit 200nm transparent conducting oxide ITO (Indium Tin Oxide) film directly on n^+-type layer of p-i-n wires for making top electrode of the solar cell (figure 1h). After that, the samples were loaded out of the Sputtering system and the covering quartz panels were also taken out from the sample devices (figure 1k), next an area of ITO around the operation area of the cell was etched from the sample's surface via photolithography process to complete the solar cell devices (figure 1*l*), notice that a part of ITO outside of p-i-n wires area on the sample's surface was unremoved as figure 1m for top contact of the solar cell, this helps to take electrical measurement of the cells easily. The cell was then measured the electrical properties under 1 Sun-AM 1,5G (1000W/m^2) with Solar simulator system.

3. RESULTS AND DISCUSSION

3.1 Scanning electron microscope observations of Al-catalyzed SiNWs and p-i-n wires -factor

From SEM image (figure 2) we see that the SiNWs are highly tapered, the diameter at their top part being comparable to the wavelengths of visible light. This is an ideal situation for minimizing light reflection (see *e.g.*, ref [26]) for solar cell applications, since there is a gradual change of refractive index going from air down to the roots of the Si wires. Beside we also observed the ~ 11μm-long (on average) NWs shown on fig.2 have been grown during 40min, which corresponds to an average growth rate of ~ 275nm/min (neglecting any incubation time). Their diameter at the base lies in the 100-120nm range. Because our growth temperature is below the Al-Si eutectic temperature (577°C) [25] and since we did not perform any particular thermal treatment before growth (such as a pre-alloying at T > 577 °C, which would activate the VLS mechanism [21,22]) the SiNWs probably grew according to a VSS mechanism (instead of undercooled VLS [21]), as already reported for growth in the temperature range 430-490°C [15]. The low growth rate observed here (compared to the ~ 5μm/min claimed in ref. [22] for growth at 520°C) is another indication that NW growth follows a VSS mechanism.

As mentioned in the experiment, the process of p-i-n wires growth includes growth of p-type core SiNWs, deposition of shells (intrinsic and n^+-type a-Si), all steps were done in the same PECVD system step by step, figure 3 shows the thickness of the shells (intrinsic and n^+-type layers) was 200nm (150nm intrinsic a-Si and 50nm n^+ a-Si respectively).

As mentioned in the experiment, the process of p-i-n wires growth includes growth of p-type core SiNWs, deposition of shells (intrinsic and n^+-type a-Si), all steps were done in the same PECVD system step by step, figure 3 shows the thickness of the shells (intrinsic and n^+-type layers) was 200nm (150nm intrinsic a-Si and 50nm n^+ a-Si respectively).

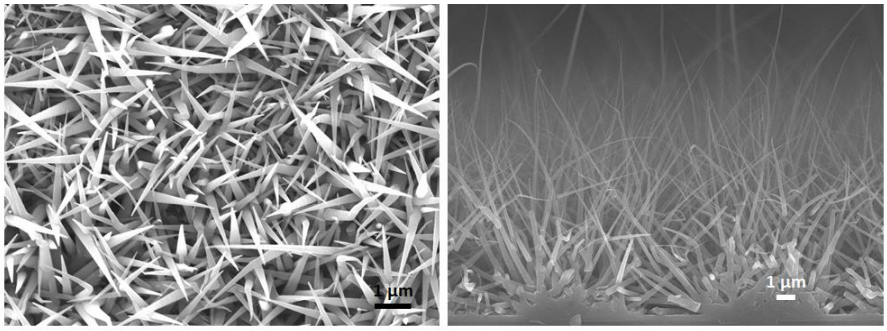

Figure 2. *Scanning electron microscope pictures of the core p-Si NWs grown on a quartz substrate at 550^{o}C.*

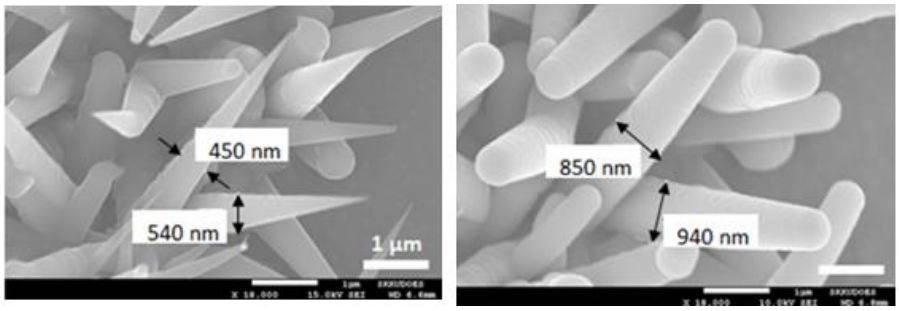

Figure 3. *Determination of the thickness of the shell layers. (a): The core Al-doped Si wires right after growth. (b): After deposition of the intrinsic and n^+ a-Si:H shell. All the scanning electron microscope (SEM) pictures are taken at the same place. The bar scale is 1 µm on all pictures.*

3.2. Structural characterizations of p-type core Al-catalyzed SiNWs grown on quartz substrates (550°C)

Figure 4c shows an electron diffraction pattern, which can be indexed with the help of a recent paper [27]. The extra features in the diffraction pattern are the result of both microtwins which induce extra spots by double diffraction, and nanotwins which induce some streaking effects [27]. Figure 4b shows a high resolution TEM image of a SiNW; there seems to be a regular superstructure, but this is only the result of a Moiré pattern induced by the presence of nanotwins in the SiNW, figure 5 explained clearly about this phenomenon. Again, our observations are totally consistent with the

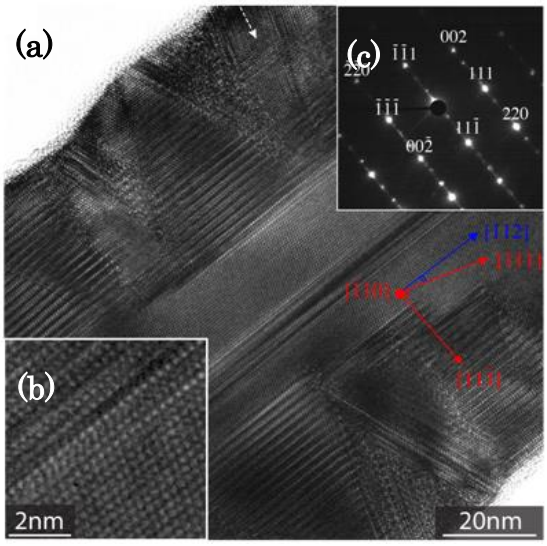

Figure 4. *HRTEM image of a SiNW showing high concentration of nanotwins; those induce the formation of Moiré patterns which looks like a superstructure.*

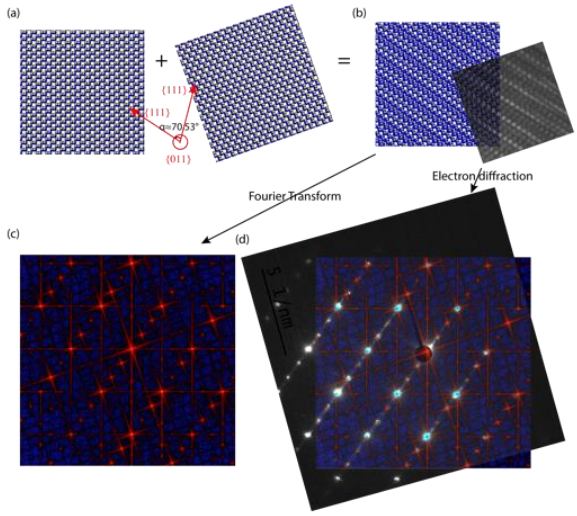

Figure 5*. Simulation of the SiNWs Moiré structure: (a) Two silicon (111) surface tilted from 70.53°, (b) When the 2 images of (a) are superimposed, a Moiré structure naturally appears, which corresponds to the structure observed in TEM image at figure 4b, (c) A Fast Fourier Transform of the "simulated" Moiré structure (d) superimposed with the electron diffraction pattern of the Moiré structure measured in TEM. The superposition of two (111) surface tilted from 70.53° reproduces all the features observed in the TEM image.*

3.3. Electrical characterizations of the Al-catalyzed SiNWs.

In the experiment session, we mentioned in detail how to prepare a transistor device (figure 6) to measure electrical characterizations of the p-type core Al SiNWs, various transistor characteristics of the Si NW shown on figure 7, when the highly doped Si substrate is used as a back gate. The drain current (I_{DS}) is clearly seen to decrease as the gate voltage (V_{GS}) goes from negative to positive values, which is indicative of a p-type behavior (figure 7a). The output characteristics of the transistor are shown on figure 7b. The gate influence is very limited (the transistor cannot be turned off) and saturation is not reached, which indicates highly doped, metal-like wires.

We have evaluated the hole mobility using the classical formula: $\mu = g_m \frac{L^2}{V_{DS} C_{tr}}$, where g_m is the transconductance of the device ($g_m = \frac{\partial I_{DS}}{\partial I_{GS}}$), L is the channel length of the transistor (here, 3µm), V_{DS} is the drain voltage (0.2V) and C_{tr} is the gate capacitance of the transistor.

Because we have a nanowire lying on a plane, the gate capacitance can be approximated by: $C_{tr} = \frac{2\pi L \varepsilon_0 \varepsilon_r}{Ln(4t_{0x}/d)}$, where ε_0 is the vacuum permittivity, ε_r is the dielectric constant of the gate insulator (here, we took $\varepsilon_r \approx 2.5$, *i.e.*, an average value between air and SiO_2), t_{ox} is the thickness of the gate insulator and d is the nanowire diameter. If we take an average value of d = 190nm ({150+230}/2 figure 6), we get $C_{tr} \approx 5.60 \times 10^{-16}$ F.

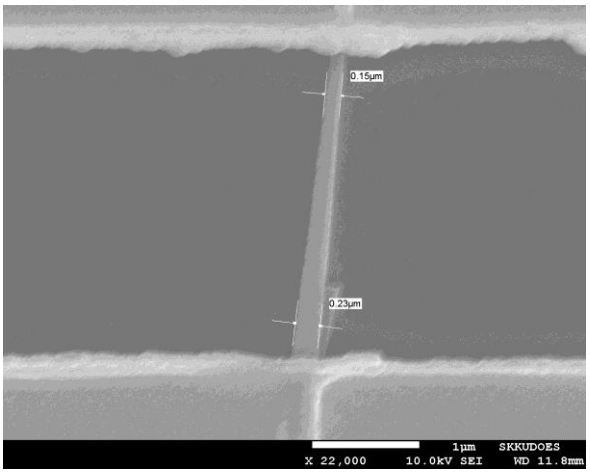

Figure 6. *A typical Si NW ready for electrical measurements. The electrode separation is 3µm. The bar scale on the picture is 1 µm. Because the Si NWs are tapered after growth, the diameter varies between ~ 150 and 230nm.*

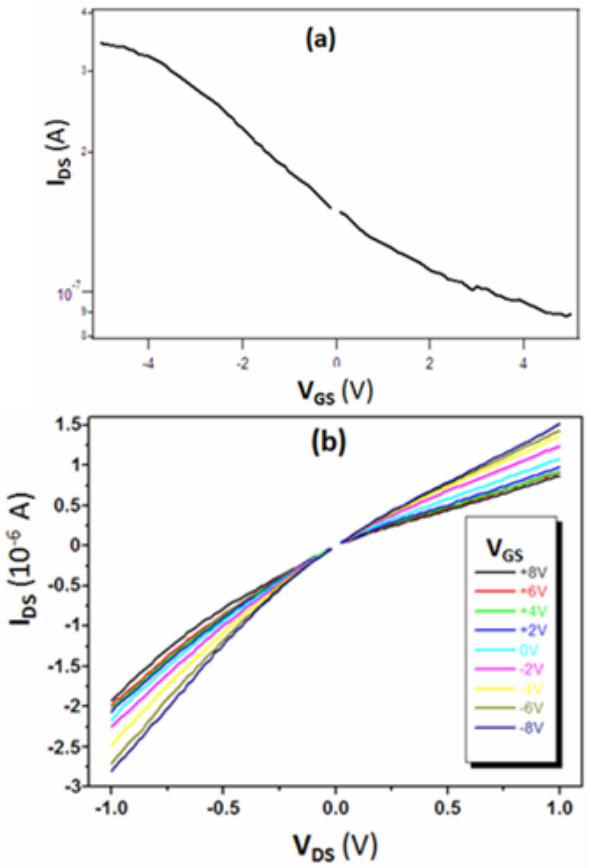

Figure 7*. Electrical characterizations of the core Si NWs. (a): Transfer characteristic, with a V_{DS} voltage of 0.2 V. (b): Output characteristics.*

The g_m value can be extracted from the slope of figure 7a; we find $g_m = \frac{\Delta I_{DS}}{\Delta I_{GS}} \approx 3.64$ x 10^{-8}A/V. With the above values, we find a hole mobility of ~ 29cm^2/Vs, for d = 190nm.

Now, the resistance of the wire can be evaluated in the voltage interval between – 50mV and + 50mV where the output characteristic for V_{GS} = 0 is linear. We find R ≈ 3.75kΩ. Still assuming a 190nm average diameter wire, this yields σ ≈ 282Ω.cm. Hence, the carrier concentration is ~ 6 x 10^{19}/cm^3. We have measured the characteristics of 4 different Si wires and found carrier concentrations between ~ 4 and 6.7 x 10^{19}/cm^3.

3.4. Application to solar cells.

Figure 8 presents the electrical characteristics of one of our best solar cell structures based on array p-i-n wires, both in the dark and under 1 sun illumination (1000W/m^2). We notice that a-Si works as a direct band gap material (in opposite way, crystalline Si (c-Si) works as an indirect band gap) so a-Si has a higher absorption index compare with c-Si, on the other hand with our structure we just used a very thin top layer of n^+-type a-Si, so most of the light is absorbed in the intrinsic a-Si:H region of the p-i-n wires. The solar cell released an open circuit voltage (V_{OC}) of ~ 0.7V, this value of V_{oc} is quite high compare with another reports about SiNWs solar cells based on a-Si shell with core-shell structure [29], thanks to our p-i-n structure's thin shells (150nm intrinsic a-Si and 50nm n^+-type), carriers in intrinsic a-Si absorption layer which were obtained by light photons were collected quickly by domestic electric field between p-type core and n^+-type layer, besides minority carriers were obtained in n^+-type layer because of light photons also diffused quickly to the electric field domain then collected by electric field before recombination. So recombination speed in our structure was limited strongly, this is the reason we had a high value of V_{oc} compare with earlier reports [26], on the other hand the band gap of the absorbtion layer (a-Si) is quite high ~ 1.7eV [30], this is also another reason for our high value of V_{oc}. The short circuit current was ~ 893.75.10^{-3}mA, so the short circuit current density (J_{SC}) under 1 sun-AM 1.5G illumination is ~ 14.3mA/cm^2 (the operation area of the cell is 0.25x0.25cm^2). The fill factor of the cell is 48.2%, this value of fill factor is still quite low, this parameter relates directly with series resistance of the cell, we suggested that space between p-i-n wires was quite close together in our

structure, so when ITO film was deposited, it could not obtain an uniform and continuous ITO film along p-i-n wires' body, this leaded to a high series resistance, then resulted in a low fill factor [31,32]. We can overcome this phenomenon by optimizing density of nanowires (via annealing Al film before growth) for obtaining a good spacing between p-i-n wires before ITO film coating.

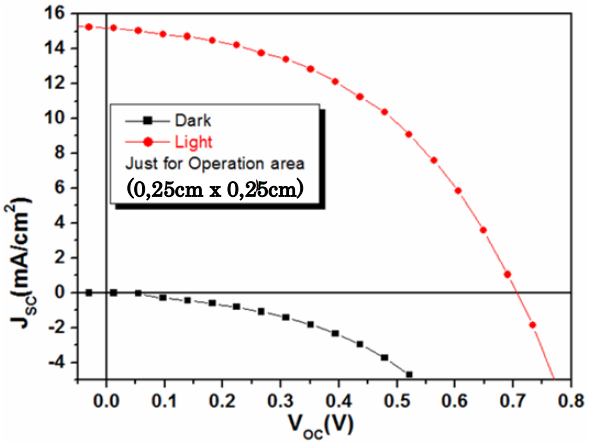

Figure 8. *Current–voltage (J–V) characteristics of the p-i-n radial junction silicon nanowire (SiNW) solar cell.*

4. CONCLUSSION

Al-catalyzed SiNWs were successfully fabricated via a VSS mechanism in the PECVD reactor at 550 °C and their various properties evaluated. All the Al-catalyzed SiNWs that we have observed in the TEM exhibit high densities of micro- and nano-twins. From electrical characterization (field-effect transistors), we found that the Al-catalyzed SiNWs are heavily p-doped at a growth temperature of 550°C, with active dopant concentrations (Al) reaching ~ 10^{19}/cm^3. For solar cell application, solar cells were fabricated based on these high p-doped Al SiNWs released a high open circuit voltage (V_{oc}) of ~ 0.7V, the current density of ~ 14.3mA/cm^2, however the fill factor was still low (48.2%), we can improve this parameter by optimizing the density of Al SiNWs to obtain a wide enough space between p-i-n wires before ITO film coating. The processes employed to fabricate these devices are readily scalable, making this solar cell architecture a promising candidate for future photovoltaic applications.

REFERENCES

[1] B.M. Kayes, H.A. Atwater, N.S. Lewis, *Comparison of the device physics principles of planar and radial p-n junction nanorod solar cells*, J. Appl. Phys. 97 (2005) 114302.

[2] B.M. Kayes, M.A. Filler, M.C. Putnam, M.D. Kelzenberg, N.S. Lewis, H.A. Atwater, *Growth of vertically aligned Si wire arrays over large areas (>1cm2) with Au and Cu catalysts*, Appl. Phys. Lett. 91 (2007) 103110.

[3] M.C. Putnam, S.W. Boettcher, M.D. Kelzenberg, D.B. Turner-Evans, J.M. Spurgeon, E.L. Warren, R.M. Briggs, N.S. Lewis, H.A. Atwater, *Si microwire-array solar cells*, Energy Environ. Sci. 3 (2010) 1037–1041.

[4] M.D. Kelzenberg, D.B. Turner-Evans, M.C. Putnam, S.W. Boettcher, R.M. Briggs, J.Y. Baek, N.S. Lewis, H.A. Atwater, *High-performance Si microwire photovoltaics*, Energy Environ. Sci. 4 (2011) 866–871.

[5] M.D. Kelzenberg, S.W. Boettcher, J.A. Petykiewicz, D.B. Turner-Evans, M.C. Putnam, E.L. Warren, J.M. Spurgeon, R.M. Briggs, N.S. Lewis, H.A. Atwater, *Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications*, Nat. Mater. 9 (2010) 239–244.

[6] X. Li, Z. Chen, N. Shen, D. Sarkar, N. Singh, K. Banerjee, G.-Q. Lo, D.-L. Kwong, *Vertically Stacked and Independently Controlled Twin-Gate MOSFETs on a Single Si Nanowire*, IEEE Electron Device Lett. 32 (2011) 1492–1494.

[7] K.H. Cho, K.H. Yeo, Y.Y. Yeoh, S.D. Suk, M. Li, J.M. Lee, M.-S. Kim, D.-W. Kim, D. Park, B.H. Hong, Y.C. Jung, S.W. Hwang, *Experimental evidence of ballistic transport in cylindrical gate-all-around twin silicon nanowire metal-oxide-semiconductor field-effect transistors*, Appl. Phys. Lett. 92 (2008) 52102.

[8] J.-P. Colinge, C.-W. Lee, A. Afzalian, N.D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, R. Murphy, *Nanowire transistors without junctions*, Nat. Nanotechnol. 5 (2010) 225–229.

[9] G. Lehoucq, P. Bondavalli, S. Xavier, P. Legagneux, P. Abbyad, C.N. Baroud, D. Pribat, *Highly sensitive pH measurements using a transistor composed of a large array of parallel silicon nanowires*, Sens. Actuators B Chem. 171–172 (2012) 127–134. doi:10.1016/j.snb.2012.01.054.

[10] D.V. Talapin, H. Yu, E.V. Shevchenko, A. Lobo, C.B. Murray, *Synthesis of Colloidal PbSe/PbS Core−Shell Nanowires and PbS/Au Nanowire−Nanocrystal Heterostructures*, J. Phys. Chem. C. 111 (2007) 14049–14054.

[11] L. Zhu, M.R. Phillips, C. Ton-That, *Coalescence of ZnO nanowires grown from monodisperse Au nanoparticles*, CrystEngComm. 17 (2015) 4987–4991.

[12] S. Misra, L. Yu, W. Chen, M. Foldyna, P.R. i Cabarrocas, *A review on plasma-assisted VLS synthesis of silicon nanowires and radial junction solar cells*, J. Phys. Appl. Phys. 47 (2014) 393001.

[13] T.I. Kamins, R.S. Williams, Y. Chen, Y.-L. Chang, Y.A. Chang, *Chemical vapor deposition of Si nanowires nucleated by TiSi2 islands on Si*, Appl. Phys. Lett. 76 (2000) 562–564.

[14] S. Hofmann, R. Sharma, C.T. Wirth, F. Cervantes-Sodi, C. Ducati, T. Kasama, R.E. Dunin-Borkowski, J. Drucker, P. Bennett, J. Robertson, *Ledge-flow-controlled catalyst interface dynamics during Si nanowire growth*, Nat. Mater. 7 (2008) 372–375.

[15] Y. Wang, V. Schmidt, S. Senz, U. Gösele, E*pitaxial growth of silicon nanowires using an aluminium catalyst*, Nat. Nanotechnol. 1 (2006) 186–189.

[16] O. Moutanabbir, D. Isheim, H. Blumtritt, S. Senz, E. Pippel, D.N. Seidman, *Colossal injection of catalyst atoms into silicon nanowires*, Nature. 496 (2013)

[17] D.E. Perea, E.R. Hemesath, E.J. Schwalbach, J.L. Lensch-Falk, P.W. Voorhees, L.J. Lauhon, *Direct measurement of dopant distribution in an individual vapour–liquid–solid nanowire*, Nat. Nanotechnol. 4 (2009) 315–319.

[18] J.E. Allen, D.E. Perea, E.R. Hemesath, L.J. Lauhon, *Nonuniform Nanowire Doping Profiles Revealed by Quantitative Scanning Photocurrent Microscopy*, Adv. Mater. 21 (2009) 3067–3072.

[19] H. Schmid, M.T. Björk, J. Knoch, S. Karg, H. Riel, W. Riess, *Doping limits of grown in situ doped silicon nanowires using phosphine*, Nano Lett. 9 (2009) 173–177.

[20] Y. Ke, X. Weng, J.M. Redwing, C.M. Eichfeld, T.R. Swisher, S.E. Mohney, Y.M. Habib, *Fabrication and Electrical Properties of Si Nanowires Synthesized by Al Catalyzed Vapor−Liquid−Solid Growth*, Nano Lett. 9 (2009) 4494–4499.

[21] B.A. Wacaser, M.C. Reuter, M.M. Khayyat, C.-Y. Wen, R. Haight, S. Guha, F.M. Ross, *Growth system, structure, and doping of aluminum-seeded epitaxial silicon nanowires*, Nano Lett. 9 (2009) 3296–3301.

[22] S.-Y. Choi, W.Y. Fung, W. Lu, *Growth and electrical properties of Al-catalyzed Si nanowires*, Appl. Phys. Lett. 98 (2011) 33108.

[23] T.I. Kamins, R.S. Williams, D.P. Basile, T. Hesjedal, J.S. Harris, *Ti-catalyzed Si nanowires by chemical vapor deposition: Microscopy and growth mechanisms*, J. Appl. Phys. 89 (2001) 1008–1016.

[24] S.J. Whang, S.J. Lee, W.F. Yang, B.J. Cho, Y.F. Liew, D.L. Kwong, *Complementary Metal-Oxide-Semiconductor Compatible Al-Catalyzed Silicon Nanowires*, Electrochem. Solid-State Lett. 10 (2007) E11. doi:10.1149/1.2716304.

[25] O. Moutanabbir, S. Senz, R. Scholz, M. Alexe, Y. Kim, E. Pippel, Y. Wang, C. Wiethoff, T. Nabbefeld, F. Meyer zu Heringdorf, M. Horn-von Hoegen, *Atomically Smooth p-Doped Silicon Nanowires Catalyzed by Aluminum at Low Temperature*, ACS Nano. 5 (2011) 1313–1320.

[26] E.C. Garnett, M.L. Brongersma, Y. Cui, M.D. McGehee, *Nanowire Solar Cells*, Annu. Rev. Mater. Res. 41 (2011) 269–295.

[27] C. Cayron, M. Den Hertog, L. Latu-Romain, C. Mouchet, C. Secouard, J.-L. Rouviere, E. Rouviere, J.-P. Simonato, *Odd electron diffraction patterns in silicon nanowires and silicon thin films explained by microtwins and nanotwins*, J. Appl. Crystallogr. 42 (2009) 242–252.

[28] Z. He, H.T. Nguyen, L.D. Toan, D. Pribat, *A detailed study of kinking in indium-catalyzed silicon nanowires*, CrystEngComm. 17 (2015) 6286–6296.

[29] K.-Q. Peng, S.-T. Lee, *Silicon Nanowires for Photovoltaic Solar Energy Conversion*, Adv. Mater. 23 (2011) 198–215.

[30] A. Kanevce, W.K. Metzger, *The role of amorphous silicon and tunneling in heterojunction with intrinsic thin layer (HIT) solar cells*, J. Appl. Phys. 105 (2009) 94507.

[31] M.M. Adachi, M.P. Anantram, K.S. Karim, *Core-shell silicon nanowire solar cells*, Sci. Rep. 3 (2013) 1546.

[32] J. Cho, B. O'Donnell, L. Yu, K.-H. Kim, I. Ngo, P.R. i Cabarrocas, *Sn-catalyzed silicon nanowire solar cells with 4.9% efficiency grown on glass*, Prog. Photovolt. Res. Appl. 21 (2013) 77–81.

Corresponding author:
PhD. Le Duc Toan
Phu Yen University, Vietnam
E-mail: toanvatlieu@gmail.com