A DESIGN OF HIGH-EFFICIENCY PWM/PFM BUCK CONVERTER WITH BYPASS MODE USING CMOS 65NM

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ABSTRACT

This paper presents the design of high efficiency PWM/PFM Buck Converter with Bypass mode for battery-powered products. In this design, when the input voltage falls below 1.9V, the converter automatically enters Bypass mode. When input voltage rises upper 2.1V, the converter operates in PWM mode or PFM mode depending on load current. The conversion efficiency is over 85% with load current range from 2mA to 500mA. The structure in this paper also improves the capability of ZCD circuit, and eliminates the input referred offset voltage which helps to detect more accurately when the current of inductor goes to zero. Soft-start circuit also improves and merges with error amplifier to limit inrush current and avoid output voltage overshoot when power starts up. To obtain an accurate trip point to enable or disable the Buck converter, the implementation of Vdd detection circuit is based on a structure of bandgap circuit. This ensures that the trip point is as accurate as the bandgap reference voltage.

Keywords: *PWM; PFM; Bypass mode; DC-DC; Buck converter.*

1. INTRODUCTION

Sub-modules in a System On Chip can simply be classified into analog and digital circuits. This requires that each module has a special voltage regulator power supply. Hence, there is an increasing requirement to pay more attention to the power management considerations in a chip to achieve high-efficiency along with high performance in a small area. A high-efficiency DC-DC converter with a wide load current range is very important for portable communication devices. For battery-powered products, power efficiency directly affects battery life. So DC-DC converter must have a high efficiency even for the cases where the battery is either full or charging. It should also have the ability to adapt to rapid load transients. To this end, we need to use the pulse-width modulation (PWM) and pulse frequency modulation (PFM) techniques for power management purposes for effectively improving the efficiency. As we know, the PWM mode has low efficiency in light load while the PFM mode has low efficiency in high load. To increase efficiency in a wide load current range, we need to combine both controls on a converter [1]. The common issues in portable electronic devices are the voltage battery decreases with time. To exploit maximum energy from the battery, the added switch between the battery and the loading is the best way to extend the lifetime of electronic devices. Besides, when the input voltage closes to the output voltage, the duty cycle closes to 100%, the ripple and noise of the output voltage will increase. In the traditional ZCD circuit for DC-DC converter, the comparator was used to detect when the voltage at the drain of NMOS in the power stage > 0. The gap between two inputs of the comparator is only a few millivolts that means the size of NMOS impact to the result. If we decrease the size of NMOS, the comparator is easy to detect but the efficiency of the converter is also reduced. Besides that, the input-referred offset of the comparator is around 5 mv to 20 mv, so it has a strong effect to the ability detection of the ZCD circuit. To solve this issue, in this paper we applied the auto-zero technique to reduce

the offset of comparator go to smaller than 1mV. The purpose of this paper is to introduce the control scheme and the design of high-efficiency Buck converter with an automatic transition between PWM mode, PFM mode, and Bypass mode, it also prevents the increase of output ripple voltage and noise [2]-[3]-[4]. The organization of this paper is shown as follows. Section 2 introduces the design of PWM/PFM Buck converter with Bypass mode. The circuit analysis is shown in Section 3. The simulation results are presented in Section 4. Finally, The conclusion is presented in Section 5.

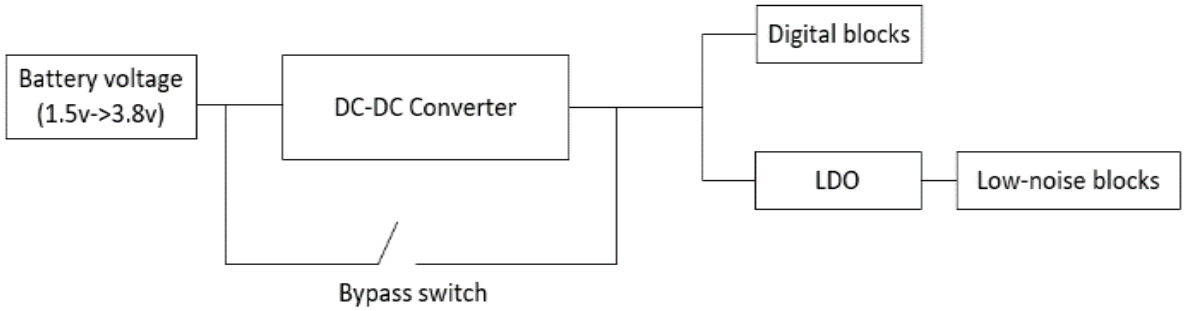

Figure 1. *Block diagram of Buck converter with bypass mode*

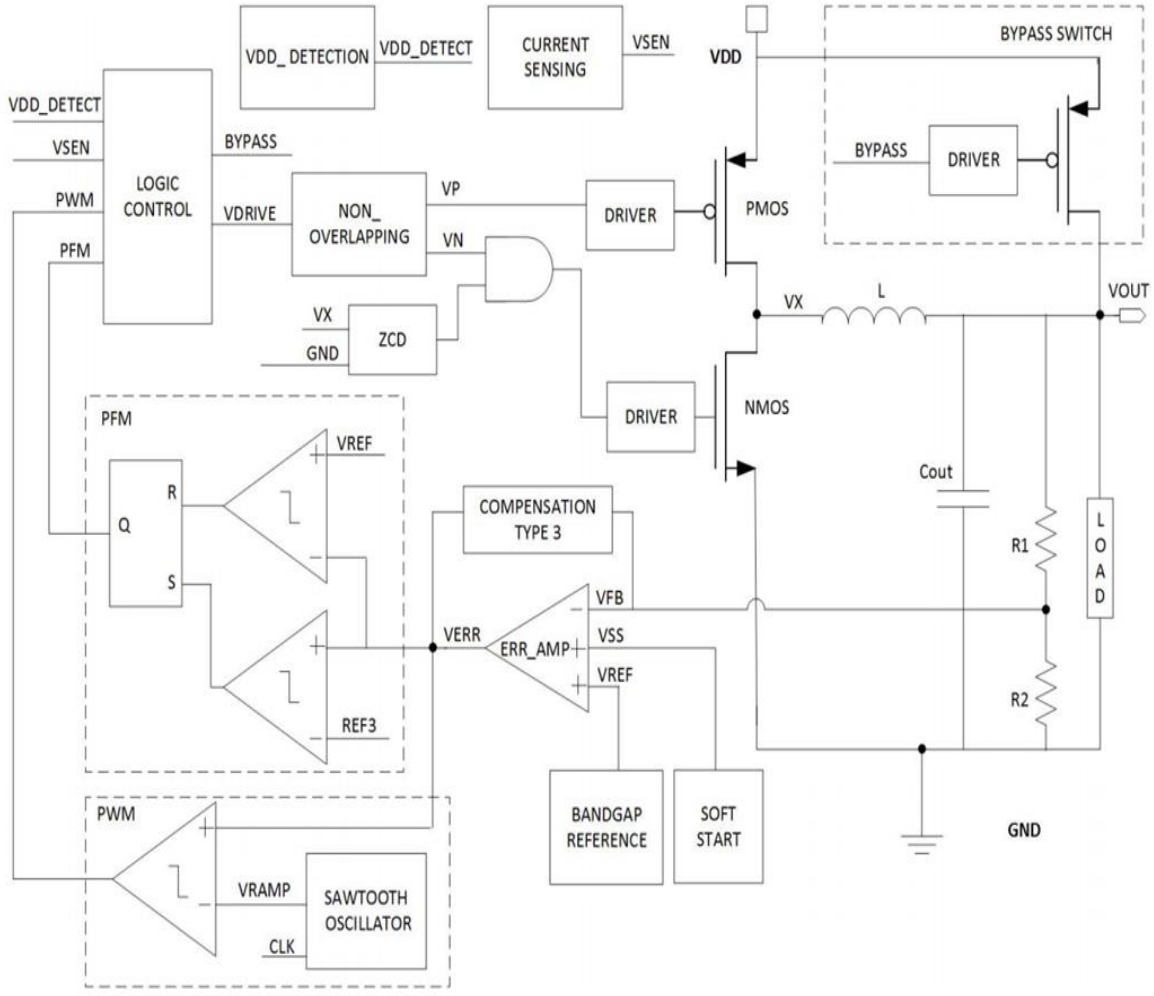

Figure 2. *Detail block diagram of the PWM/PFM Buck converter with bypass mode.*

2. PWM/PFM BUCK CONVERTER WITH BYPASS MODE

Fig. 1, Fig. 2 show the block diagram of the proposed Buck converter with a bypass switch. The voltage mode structure with the type 3 compensation is chosen to design the converter. The PWM modulator consists of a comparator and saw-tooth oscillator. VRAMP is the output of the saw-tooth oscillator, VERR is the output of the error amplifier. If VERR > VRAMP, the output of the comparator is high, the converter will turn on PMOS and turn off NMOS. If VERR < VRAMP, the converter will turn off PMOS and turn on NMOS.

The PFM modulator consists of two comparators and an SR flip-flop. The REF3 is the output voltage of the voltage divider circuit, VREF is the output of the Bandgap reference circuit (0.8V). The VERR changes with the changing of the output voltage. If VERR > REF3, the output Q of SR Flip Flop is set high and turns on PMOS; if VERR < VREF, the SR Flip Flop resets Q to low. This process is somehow like a hysteresis comparator.

The Non-Overlapping circuit controls the gate driving signals (VP, VN) such that the power transistors (PMOS, NMOS) do not turn-on simultaneously. The Current-Sensing circuit detects the inductor current which flows through PMOS and creates the VSEN signal. Soft-Start circuit is used in the converter to limit inrush current and avoid output voltage overshoot when the power starts up. The Vdd_Detection circuit is designed to sense the voltage level of the battery. When the battery voltage falls below 1.9V, the converter automatically enters Bypass mode. When the battery voltage rises upper 2.1v, the converter operates in PWM mode or PFM mode depending on load current. In this design, the ripple of the inductor current is 110mA. So, when the load current is smaller than 55mA, there is a reverse current which is passed through the NMOS. The reverse current is detected by a zero current detector (ZCD). The output of the ZCD turns off the NMOS to prevent current from output capacitor back to the ground. The Logic Control circuit controls the automatic transition between PWM mode, PFM mode, Bypass mode, soft-start operation, over-current protection… The Logic Control circuit is the core content in this paper. The more details of Logic Control circuit are shown in Section 3.

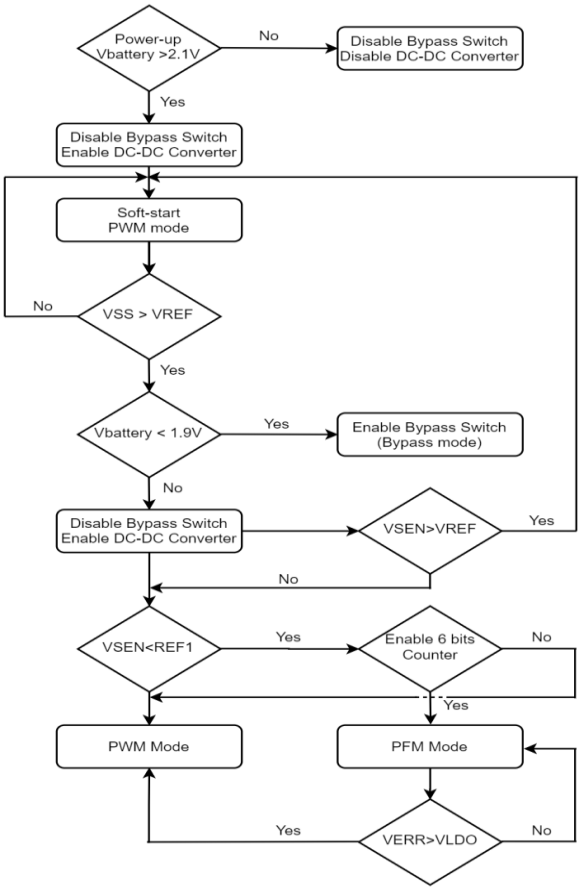

Figure 3. *Circuit Operation Flow Chart*

In soft-start operation, Buck converter is forced to enter PWM mode. After that, Buck converter operates in PWM mode or PFM mode depending on inductor current.

3. CIRCUIT ANALYSIS

3.1 Logic Control Circuit

Fig. 3 shows the operation flow chart of the converter.

When power starts up, the Vdd_Detection circuit detects the battery voltage. If the battery voltage rises to start-up level (2.1V), the Buck converter starts

operating. First, the converter enters soft-start operation and operates in PWM mode. The Bypass Switch cannot operate until finishing soft-start operation to prevent the inrush current through Bypass Switch. VSS is compared with VREF to know when the soft-start operation finishes.

Fig. 4 shows the Logic Control circuit that performs as the flow chart in Fig.3

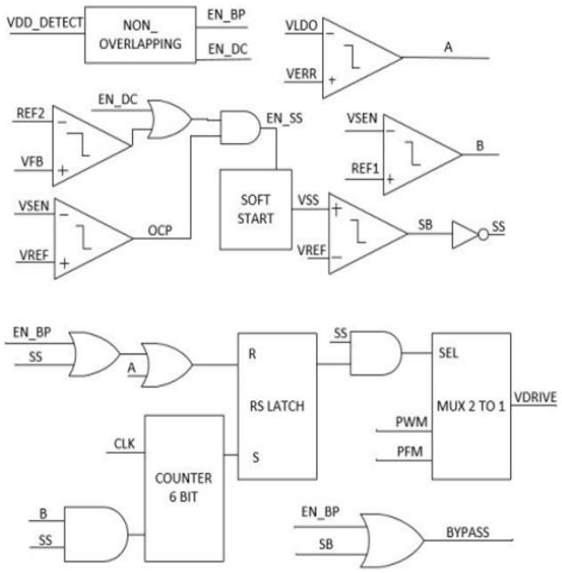

Figure 4. *Logic Control Circuit*

The inductor current is sensed by the Current-Sensing circuit. VSEN is compared with REF1 to know when inductor current is smaller than 55mA. The REF1 is the output voltage of the voltage divider circuit. If inductor current is smaller than 55mA in 64 clocks, the Buck converter changes from PWM mode to PFM mode. In PFM mode, if VERR > VLDO, the Buck converter goes back to the PWM mode. VLDO is the output voltage of Always-on LDO. VSEN is also compared with VREF to know when the inductor overcurrent occurs. If VSEN>VREF, the converter will be reset. Then, the soft-start operation performs immediately. In this design, the inductor overcurrent is 600mA. When the battery voltage goes down to 1.9V, the converter enters bypass mode. VFB is compared with REF2 to make sure that the Buck converter does not enter soft-start operation when the converter changes from Bypass mode to others mode. So, the output voltage is stable. The non-overlapping circuit controls the PMOS and Bypass Switch not to turn on simultaneously. In a transceiver, Buck converter is used for the high-efficiency conversion. LDOs are used for supplying the low ripple and low noise voltage to other circuits of the transceiver such as PLL, LNA, PA... Besides, there is an Always-on LDO that always supplies voltage to the Digital Logic Control circuit. In this Buck converter design, we take the voltage from Always-on LDO (VLDO) for creating some reference voltages. REF1, REF2, REF3 are created by the voltage divider. The value of REF1, REF2, REF3, VLDO are respectively 0.1V, 0.4V, 1.1V and 1.2V.

3.2 Soft Start and Error Amplifier Circuits

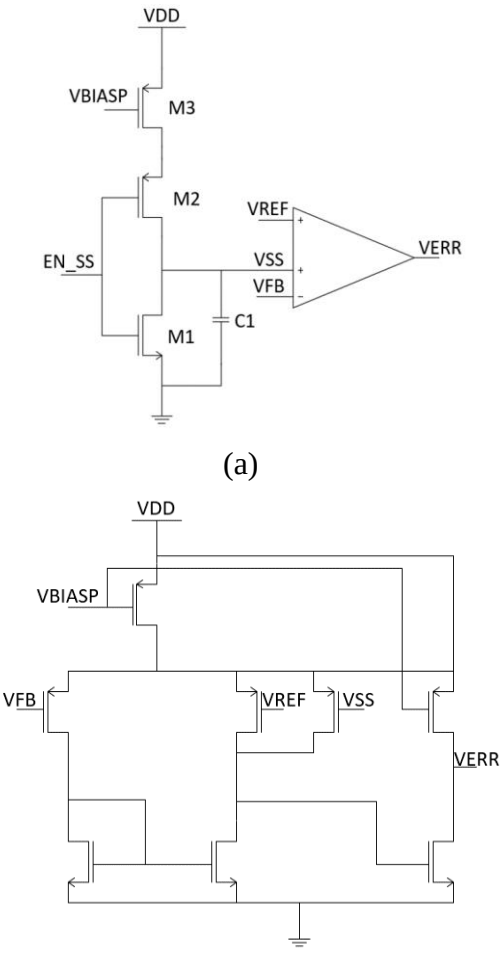

Figure 5. *(a) Soft-Start Circuit (b) Error Amplifier Circuit*

The soft-start circuit and the error amplifier circuits are shown in Fig. 5. The soft-start circuit is used in Buck converter to limit inrush current and avoid output voltage overshoot when the power starts up. The principle of soft-start is based on a linear ramp-up reference and error amplifier [5]. When the signal enable (EN_SS) is on, C_1 is charged linearly by a current reference and VSS goes up. When VSS is larger than VREF, the soft-start operation will be finished.

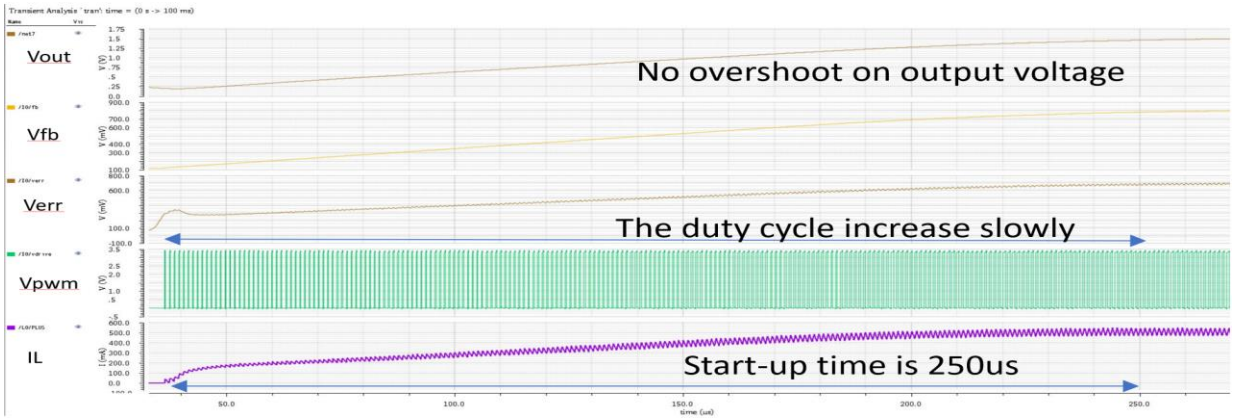

Figure 6. *The waveform of Buck converter in power-up*

3.3 Vdd_detection Circuit

Because noise from power supply can make the Vdd_Detection circuit has wrong function, it can disable DC-DC converter when VDD has a spike [6]. A hysteresis of ~ 200mV was used to improve the accuracy of Vdd_Detection circuit. The low-to-high threshold to enable DC-DC converter is 2.1V and The high-to-low threshold to disable DC-DC converter is 1.9V.

The circuit in Fig. 7 is a modification of the bandgap reference circuit. A current proportional to the supply voltage is injected into Vdd_Detection core. When the supply voltage is lower than the low-switching point (1.9V), resulting in V2 < V1 and the output of the comparator is low. When the supply voltage rises, if the supply voltage is higher than the high switching point (2.1V), the output of the comparator changes to high. The hysteresis range is 200mV

3.4 Zero-crossing detector

The ZCD circuit can prevent the output capacitor discharge which will reduce the efficiency of converter [7]. The function of ZCD is to turn off the power stage of NMOS (PMOS is closed already) when Iout is small in the Buck converter is in Discontinue Conduction Mode. The main problem with ZCD, it usually suffers from the offset caused by comparator's time delay and input referred offset voltage.

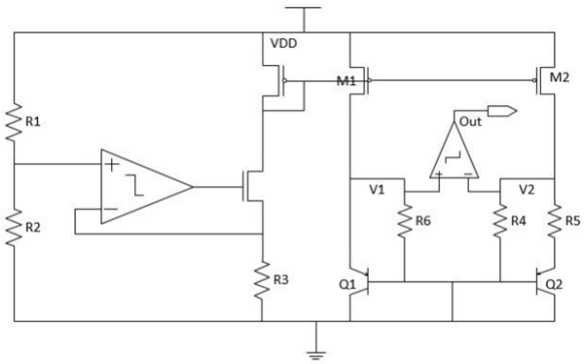

Figure 7. *Vdd detect circuit*

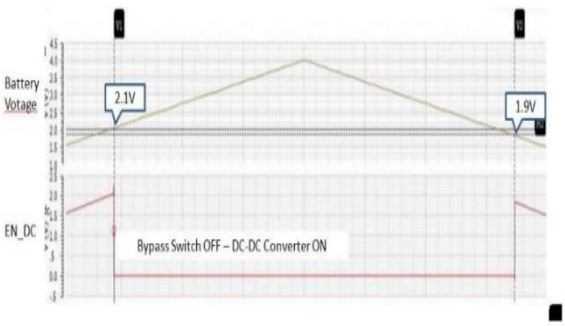

Figure 8.*The waveform of Vdd_Detect circuit*

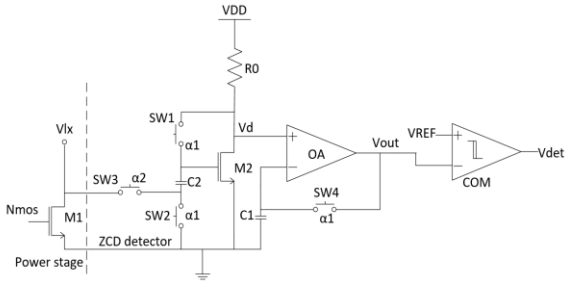

Figure 9. *Zero-crossing detector circuit*

Fig. 9 shows the structure of low offset ZCD, this operational amplifier OA can behave either as the voltage follower during the memorization phase or as the open-loop comparator during the evaluation phase. The comparator COM is used to create the signal Vdet for turn-off NMOS, the offset voltage in this structure is dominant on OA. This configuration is to provide a very fast comparison with zero input-referred offset. This is because C_1 is charged to a constant voltage $V_{C1} = V_{d(\alpha 1)} + V_{OS}$ (V_{OS} is referred to the offset of OA). The zero input voltage is detected when $V_{d(\alpha 2)}$ reaches to $V_{d(\alpha 1)}$. As the capacitor $C1$ memorizes the steady-state voltage $V_{d(\alpha 1)}$, the detection is ideally provided immediately with zero input-referred offset.

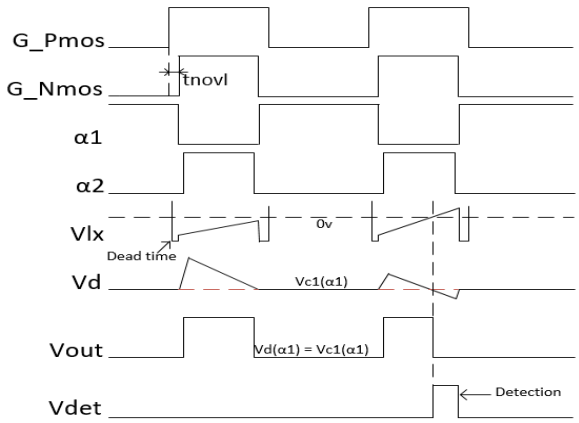

Figure 10. *Timing diagram of ZCD circuit*

The timing diagram is shown in Fig. 10. During the memorization phase α_1 (PMOS is on), the circuit sample zero (reference) input voltage. Switches SW_1, SW_2, and SW_4 are ON, whereas switch SW_3 is OFF. Capacitor C_2 is charged to a constant voltage $V_{d(\alpha 1)}$ Thanks to the operational amplifier configured as the voltage follower, voltage $V_{d(\alpha 1)} + V_{OS}$ is also memorized in the second capacitor C_1. The evaluation phase α_2 starts slightly after the Power-NMOS turns ON (few nanoseconds). This allows us to avoid generation of an erroneous detection during the noisy power-stage switching (see Section V-A). During this phase, switches SW_1, SW_2, and SW_4 are disconnected, and SW_3 connects the bottom plate of C_1 to power-stage output voltage $V_{ON(n)} = V_{LX}$. The open switch SW_1 configures the transistor M_2 as an amplifier, whereas the open switch SW_4 allows us to operate the operational amplifier as the open-loop comparator with (+) terminal connected to V_{C2}. Referring to Fig. 8 where the $V_{ON(n)}$ voltage is negative at the beginning of the NMOS conduction, M_2 gate voltage is lower than the steady-state voltage $V_{GS}(M_2, \alpha_1)$. On this account, transistor M_2 drives less current than $I_0(\alpha_1)$, and its drain voltage V_d increases. When $V_{d(\alpha 2)} > V_{C1} + V_{OS}$, the comparator output is set to high. As soon as the input $V_{ON(n)}$ voltage reaches zero and becomes positive, the $V_{d(\alpha 2)} < V_{C2} + V_{OS}$ and comparator switch the output to L. This signifies that zero-inductor current crossing occurred. As already mentioned, the identical offset V_{OS} is present in the voltage follower and comparator mode of OA. It results that the operational amplifier behaves as an auto-zero comparator, and its offset V_{OS} has no impact on the detection accuracy.

4. SIMULATION RESULTS

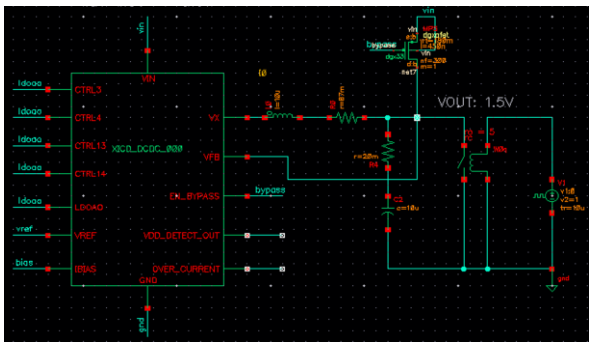

Figure 11. *The simulation set up for DC-DC converter*

We use the software Cadence to design and simulate the whole system. The CMOS models for simulation are TT, FF, SS to cover the change of PVT can affect to the performance of DC-DC converter. Fig.11 shows the simulation set-up, the inductor I_0 and capacitor C_2 are off chip, the others are on chip.

Fig. 6 shows the waveform of the Buck converter at power-up. V_{out} is an output voltage, V_{fb} is feedback of error amplifier, V_{err} is an output of error amplifier, V_{pwm} uses to drive the power MOSFETs, I_l is an inductor current. V_{fb} is charged slowly by the soft-start circuit and it limits the inductor current, no overshoot at power-up. V_{pwm} shows the duty cycle of Buck converter at power-up, we can see the duty cycle increase step by step to limit the inductor current and avoid the overshoot on output voltage.

Fig. 8 shows the simulation result of Vdd_Detect circuit. When the battery voltage is smaller than 1.9V, EN_DC signal is high. So, the Bypass Switch is ON and the Buck converter is OFF. When the battery voltage is larger than 2.1V, the Bypass Switch is OFF and the Buck converter is ON.

Fig. 12 shows the operation of converter in PWM mode, Bypass mode and PFM mode. First, the converter enters soft-start operation and operates in PWM mode. After finishing soft-start operation, the converter continues operating in PWM mode because the load current (ILOAD) is 350mA. When the battery voltage is smaller than 1.9V, the converter enters Bypass mode. In this case, the output voltage depends on the input voltage and the dropout voltage of Bypass Switch. When the ILOAD = 10mA, the converter changes to PFM mode automatically.

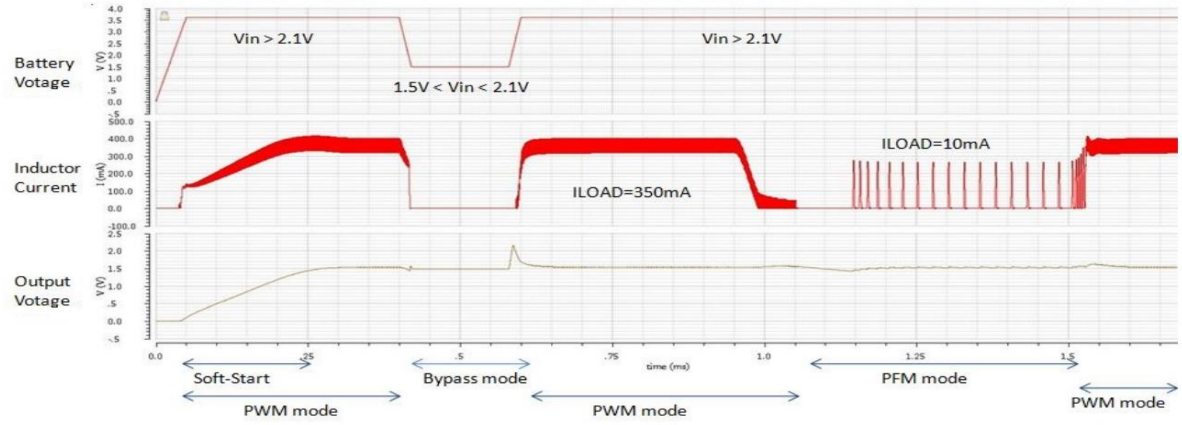

Figure 12. *Transition between Bypass mode, PWM mode and PFM mode*

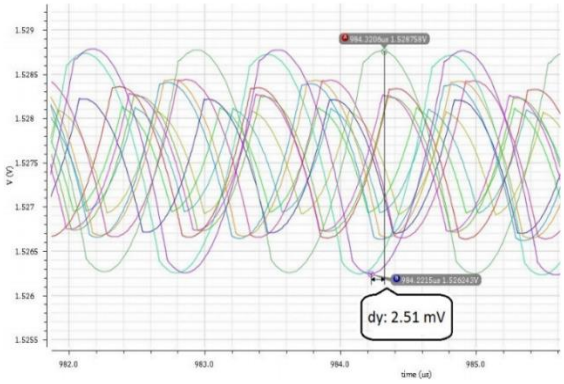

Figure 13. *The variation of the output voltage over process-temperature in PWM mode*

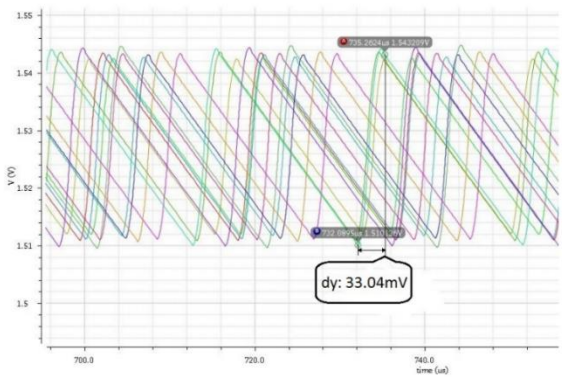

Figure 14. *The variation of the output voltage over process-temperature in PFM mode*

Fig. 13 and Fig. 14 show the variation of the output voltage over process-temperature in PWM mode and PFM mode. The ripple of output voltage is 2.5mV in PWM mode (at ILOAD=350mA) and 33mV in PFM mode (at ILOAD=10mA). PFM mode has more noise than PWM mode.

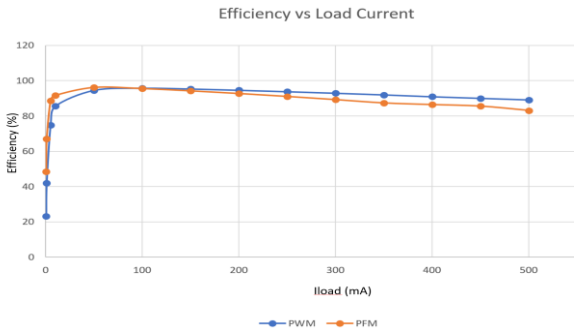

Figure 15. *The Efficiency of Buck Converter*

The conversion efficiency is over 85% with load current range from 2mA to 500mA show in Fig 15.

5. CONCLUSION

The PWM/PFM Buck Converter with Bypass mode has been implemented with a 65nm CMOS process. The conversion efficiency is over 85% with load current range from 2mA to 500mA. The structure in this paper also improves the capability of ZCD circuit, eliminates the input referred offset voltage which helps to detect more accurately when the current of inductor goes to zero. Soft-start circuit also improves and merges with error amplifier to limit inrush current and avoid output voltage overshoot when power starts up.

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